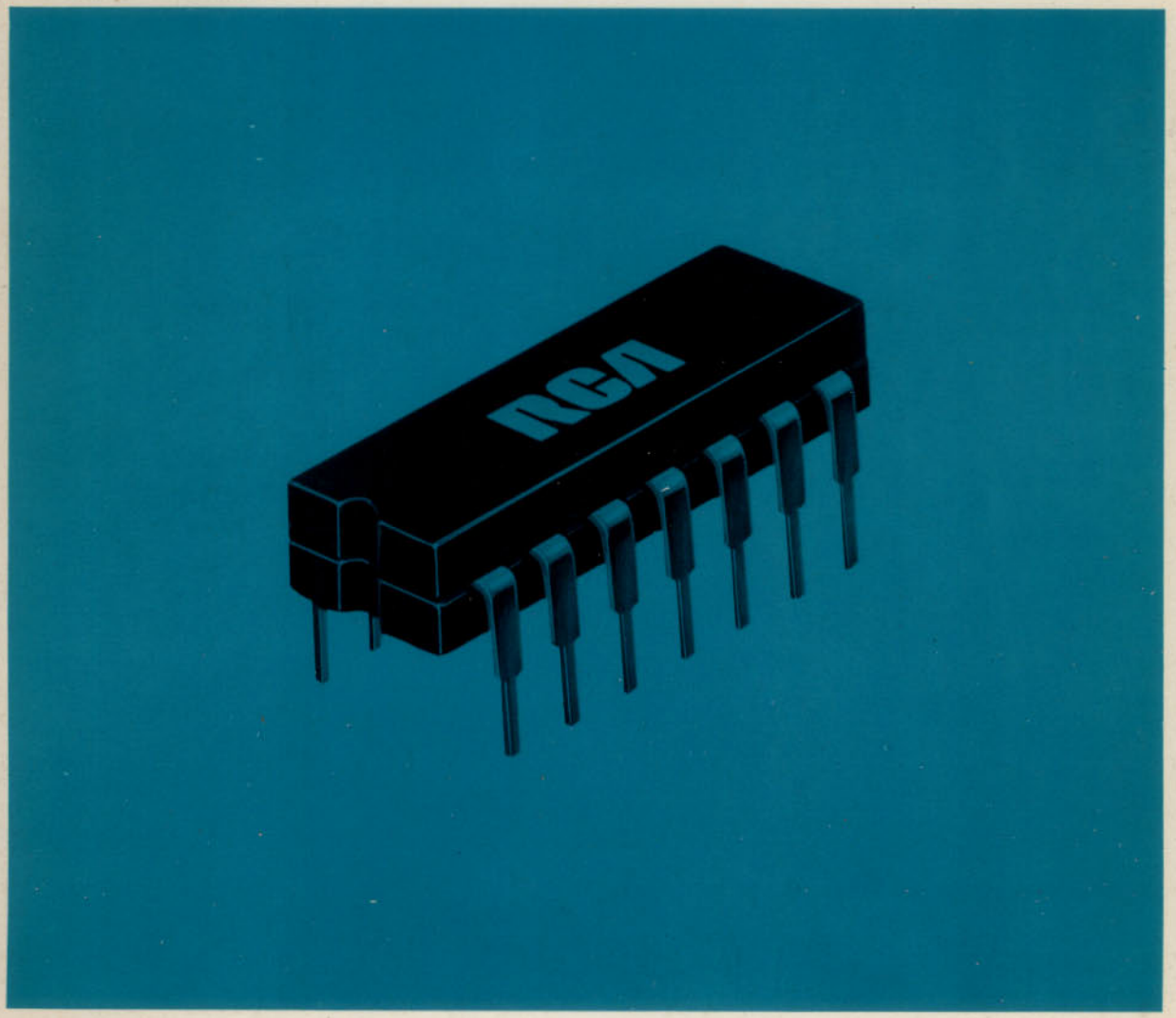
RCA Solid State

COS/MOS Integrated Circuits Manual



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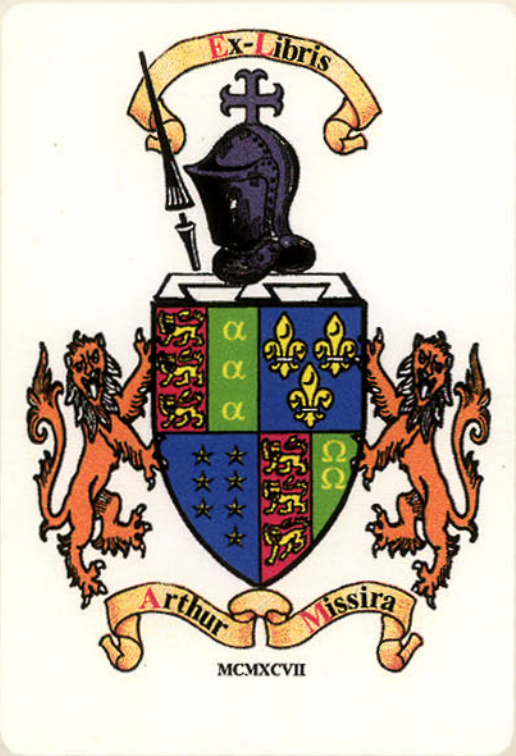
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COS/MOS Integrated Circuits Manual

COS/MOS (Complementary-Symmetry Metal-Oxide Semiconductor) devices were developed at the RCA David Sarnoff Research Laboratories in Princeton, New Jersey, in the early 1960's. The first commercial series of integrated COS/MOS circuits was announced by the RCA Solid State Division in 1968.

COS/MOS made possible orders-of-magnitude reduction in the power consumption of digital logic circuits. Perhaps the most dramatic demonstration of the potential of this new technology was the development, in 1970, of a totally new consumer product - the digital wrist watch. Battery-powered and quartz-crystal-controlled, this watch was an achievement in accuracy and compactness made possible only by COS/MOS integrated-circuit technology.

Today, the original series of COS/MOS integrated circuits has been expanded with increasingly complex designs, so that virtually any digital logic system can be implemented with commercially available packaged units. This Manual is intended as a guide to COS/MOS integrated circuits for the systems engineer and logic designer. It discusses the basic principles involved in the design and application of COS/MOS digital integrated circuits, and describes many of the circuit building blocks, ranging from basic NOR and NAND gates to complex phase-locked loops and rate multipliers.

Although this Manual is intended primarily for circuit and system designers working with solid-state circuits, it will also be useful to educators, students, radio amateurs, hobbyists, and others interested in the use of semiconductor devices and circuits.

RCA Solid State

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I. COS/MOS Integrated Circuit Fundamentals

COS/MOS (Complementary-Symmetry MOS) integrated circuits provide a number of significant advantages as compared to integrated circuits using bipolar or single-channel MOS (PMOS or NMOS) technology. These advantages include ultra-low power dissipation (microwatt level), high noise immunity (30 percent of supply voltage), and the use of a single power supply with a wide operating-voltage range (the recommended range is 3 to 18 volts; the maximum rating for B-series devices is 3 to 20 volts).

COS/MOS devices are voltage-controlled switches that have a high input impedance. They differ in both fabrication and operation from bipolar transistors, which are low-impedance current-switched devices. Although more devices are required to implement logic in COS/MOS than in single-channel MOS, COS/MOS circuits operate faster and require only a single 'clock' or control signal.

BASIC MOS TRANSISTORS

Every MOS transistor has three basic parts: the gate, the source diffusion, and the drain diffusion, as shown in Fig. 1. The gate acts as a control electrode to increase or decrease conduction in the channel between the source and drain diffusions.

All MOS transistors used in COS/MOS integrated circuits are enhancement-mode types. In this type, the transistors remain in the "off" state with a bias of zero volts from gate to source. To turn the transistors "on", conduction must be "enhanced" by application of a bias voltage of the proper polarity to the gate electrode.

There are two types of MOS transistors: n-channel (electron conduction) and p-channel ("hole" conduction).

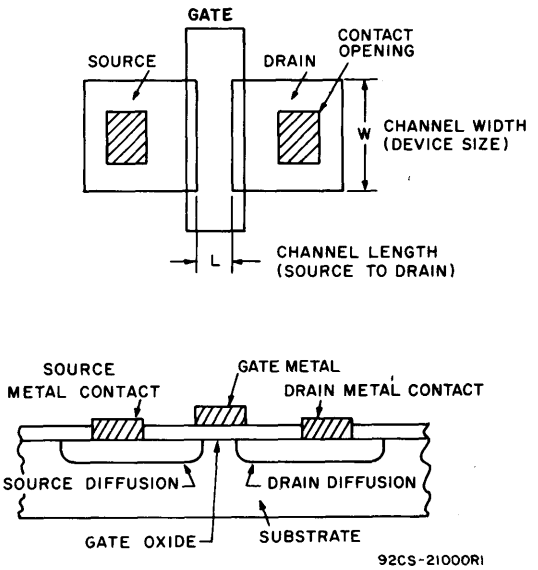


Fig. 1 — Cross-section views of a typical MOS transistor.

N-Channel Types

In n-channel MOS transistors, two heavily doped n^+ diffusions (source and drain) are closely spaced in a lightly doped p^- silicon substrate, as shown in Fig. 2(a). The metal gate is located on top of a thin insulating layer of silicon dioxide (SiO_2) directly over the channel between the diffusions.

During operation of an n-channel type, the source diffusion is connected to the substrate,

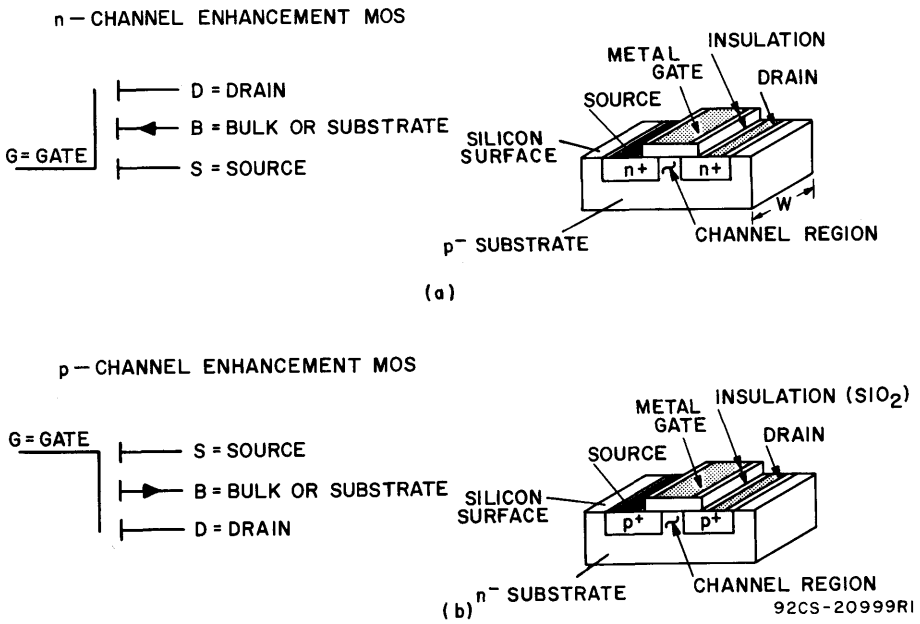


Fig. 2 – Structure of enhancement-type MOS transistors: (a) n-channel type; (b) p-channel type.

which is at the most negative potential ($-V_{SS}$). The drain diffusion is the output of the device. The impedance between the two diffusions is very high because it is the combination of back-biased diodes and the high resistance of the lightly doped substrate.

When a positive gate-to-source potential is applied, however, electrons are attracted to the channel along the surface of the silicon and form an ohmic path between the source and drain diffusions. (This action is capacitive, and no current flows through the gate electrode.)

P-Channel Types

In p-channel MOS transistors, the structure is similar, but the source and drain diffusions are heavily doped p^+ in a lightly doped n^- substrate, as shown in Fig. 2(b). In operation, the source is again connected to the substrate, which in this case is at the most positive potential ($+V_{DD}$), and the drain diffusion is the output of the device. When the gate-to-source potential is zero, the device is off and the impedance between the two diffusions is very high.

When a negative potential is applied between the gate and the source, however, positive electrical charges ("holes") are attracted to the channel along the surface of the silicon, establishing a low-resistance path.

Threshold Voltage

In both n-channel and p-channel MOS enhancement-mode devices, no current flows when the gate-to-source potential is zero. As the potential difference is increased (positive for n-channel, negative for p-channel devices), conduction starts at a point defined as the "threshold voltage" (typically 1.5 volts for both types of devices). Increasing the potential difference increases the current (i.e., reduces the drain-to-source impedance), as shown in Fig. 3. In digital

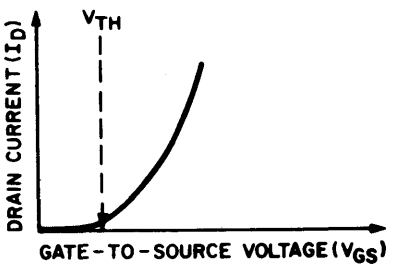


Fig. 3 – Drain current as a function of gate-to-source voltage in an MOS transistor.

operations, the voltages applied to the gates to turn transistors on are normally at the "supply rails", or the maximum levels in the system. The positive supply $+V_{DD}$ is used for n-channel conduction and the negative supply $-V_{SS}$ for p-channel conduction.

COMPLEMENTARY SYMMETRY

Because n-channel and p-channel transistors have diffusions with opposite polarity dopings, they operate with voltages of opposite polarity. That is, a positive voltage turns an n-channel device on and a p-channel device off; a negative voltage turns a p-channel device on and an n-channel device off. In COS/MOS integrated circuits, both p- and n-channel transistors are fabricated in the same semiconductor wafer, with metal connections between the paired inputs (gates) and outputs (drains), as shown in Fig. 4.

Because the gate of a COS/MOS device is essentially a capacitor (the gate metal and the substrate are the two plates, and the $Si0_2$ is the dielectric), there is no input current. When the output of one COS/MOS device drives the capacitive input of another, therefore, no IR drop occurs in the drain as a result of input current, and the output voltages are at full V_{DD} and V_{SS} levels.

Because the gates of the p-channel and n-channel pair are connected, one device must always be off regardless of the polarity of the signal on the gate. Therefore, there is never a direct path from supply to ground, and the only current from V_{DD} to V_{SS} is the very small leakage current of the MOS device that is off.

(More detailed information on device characteristics, wafer processing, and custom IC layout design is given in Chapter XIII **Custom LSI Design.**)

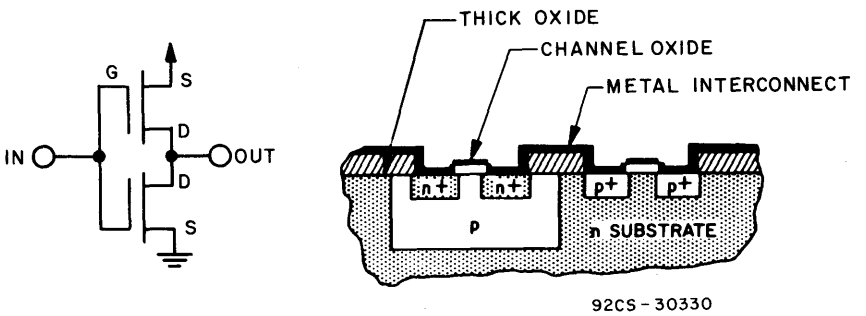


Fig. 4 — Complementary-symmetry structure used in COS/MOS integrated circuits.

II. Basic Circuit Building Blocks

This chapter describes the building-block units that form the basis for the more complex circuits discussed in the following chapters. These basic building blocks include inverters, gates, transmission gates, flip-flops, shift registers, counters, and memory cells.

INVERTERS

The n- and p-channel combination shown in Fig. 4 of the previous chapter is the inverter, the most fundamental of COS/MOS circuits. Fig. 5 shows its logic representation, simplified schematic, and truth table.

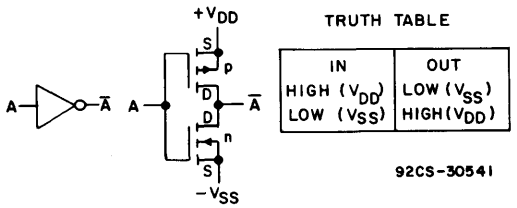


Fig. 5 — Logic diagram, simplified schematic, and truth table for a COS/MOS inverter.

A high (or positive) voltage ($+V_{DD}$) on the gate electrode turns the n-channel device on and the p-channel device off, and the output is switched to its low level ($-V_{SS}$). Similarly, a low (or negative) voltage ($-V_{SS}$) on the gate turns the p-channel device on and the n-channel device off, and the output is switched to its high level ($+V_{DD}$).

GATES

Each input to a COS/MOS gate requires a p-channel and n-channel device. In the NOR gate, the p-channel devices of the two inputs are connected in series and the n-channel devices in parallel, as shown in Fig. 6. A high

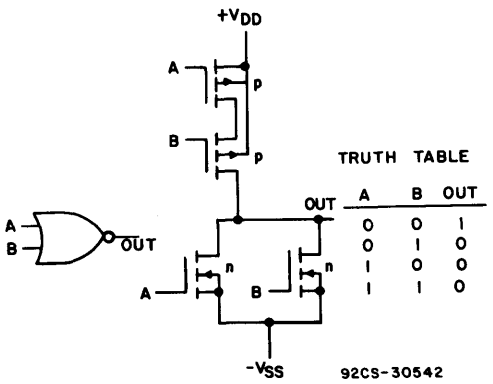


Fig. 6 — Logic diagram, simplified schematic, and truth table for a COS/MOS NOR gate.

level ($+V_{DD}$) at either input (A or B) turns the corresponding p-channel device off and n-channel device on, and the output switches to a low level ($-V_{SS}$). Both input signals (A and B) must be low in order to turn both p-channel devices on and both n-channel devices off to switch the output to a high level ($+V_{DD}$).

In the NAND gate, the n-channel devices are connected in series and the p-channel devices in parallel, as shown in Fig. 7. A low level ($-V_{SS}$) at either input (A or B) turns the corresponding n-channel device off and p-channel device on, and switches the output to $+V_{DD}$. Both inputs (A and B) must be high to turn both n-channel devices on and both p-channel devices off and switch the output to $-V_{SS}$.

Larger gates can be made by adding additional inputs (but always with a p-

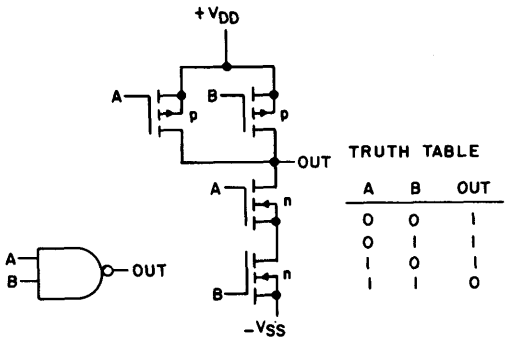


Fig. 7 – Logic diagram, simplified schematic, and truth table for a COS/MOS NAND gate.

channel and n-channel device for each input). Figs. 8 and 9 show a three-input NOR gate and a four-input NAND gate.

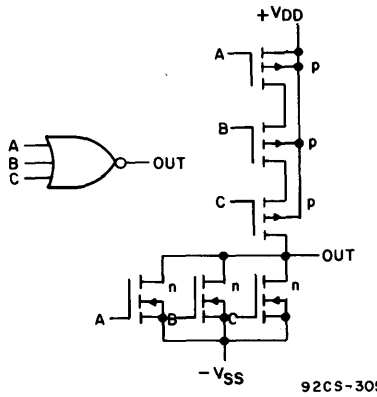


Fig. 8 – Logic diagram, simplified schematic, and truth table for a 3-input NOR gate.

RCA COS/MOS gates are commercially available in a variety of configurations, as shown in Table I. (An OR gate is simply a NOR gate with an inverter added at the output; adding an inverter to a NAND gate provides the AND function.)

If all the inputs of a particular gate are not used in a circuit, the unused inputs cannot be allowed to "float". Otherwise, any static charge accumulating at the unused high-impedance input might cause the gate potential to rise to a level which turns on both the p-channel and the n-channel devices, resulting in excessive power dissipation. For

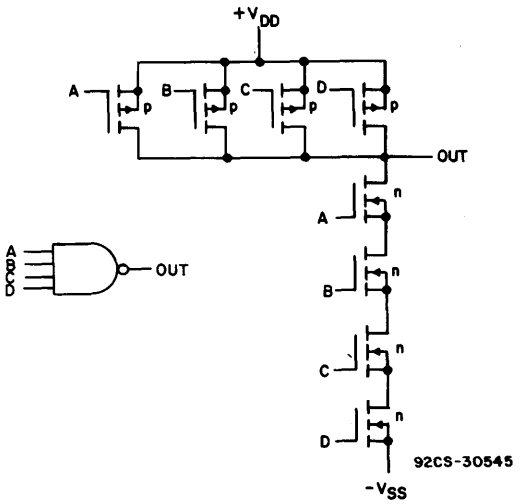


Fig. 9 – Logic diagram, simplified schematic, and truth table for a 4-input NAND gate.

example, if the eight-input CD4078 is used as a seven-input NOR gate, the unused input should be tied to $-V_{SS}$ or to one of the active inputs to assure that all the p-channel devices will be on and all the n-channel devices off when all the active inputs are low. For a NAND gate, unused inputs must be tied to $+V_{DD}$ or to an active input to assure that all n-channel devices will be on and all p-channel devices off when all active inputs are high.

Table I – Commercially Available RCA COS/MOS Gates

Gate Configuration	NOR	NAND	OR	AND
Quad 2-input	CD4001	CD4011	CD4071	CD4081
Triple 3-input	CD4025	CD4023	CD4075	CD4073
Dual 4-input	CD4002	CD4012	CD4072	CD4082
Dual 3-input plus inverter	CD4000			
Single 8-input	CD4078	CD4068		

TRANSMISSION GATES

A perfect switch is characterized by zero resistance in both the forward and reverse directions when closed and an infinite resistance in both directions when open. The COS/MOS transmission gate, with its low on-state impedance and high off-state impedance (approximately 100 megohms), is a voltage-controlled device which approaches the characteristics of the theoretical perfect switch. The transmission-gate circuit consists of an n-channel device and a p-channel device connected in parallel, as shown in Fig. 10; complementary voltages (C and $\overline{C}$) are applied to the gate electrodes.

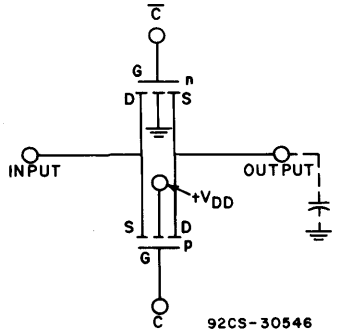


Fig. 10 – COS/MOS transmission gate.

The transmission gate provides an excellent example of how the complementary characteristics of a p-channel and n-channel pair exceed those of the individual devices. If the transmission gate were a single-channel device, it could not transmit signals over the full V_{DD} - V_{SS} voltage range. For example, assume that the supply voltage (V_{DD} - V_{SS}) is 10 volts, that the signal to be switched rises to 10 volts, and that the device used is an n-channel MOS transistor with a threshold voltage of 1.5 volts. As described in the previous chapter, conduction occurs when the gate-to-source potential exceeds the threshold voltage. With a gate signal of 10 volts and an input signal of zero, therefore, the n-channel device is on

($V_{gate\text{-}source} = 10 - 0 = 10$ V;

10 V > 1.5 V or the threshold voltage).

However, as the input signal rises to 8.5 volts, the gate-to-source potential drops to the threshold voltage

($V_{gate\text{-}source} = 10 - 8.5 = 1.5$ V),

and the device no longer conducts. Thus, the full 10-volt excursion of the input signal cannot be transmitted, as shown in Fig. 11.

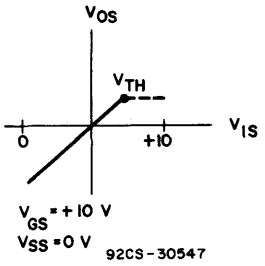


Fig. 11 – Switch characteristics of a single n-channel MOS transistor.

When a p-channel device is used in parallel with the n-channel device, and with a signal of the opposite polarity on its gate (i.e., zero volts), the p-channel is on when the input signal is 8.5 volts

($V_{gate\text{-}source} = 0 - 8.5 = -8.5$ V;

-8.5 V > -1.5 V, or the threshold voltage).

Fig. 12 shows the switch characteristics of a single p-channel device. As a result, the complementary switch does not turn off prematurely, and the full 10-volt input signal can be switched, as shown by the composite

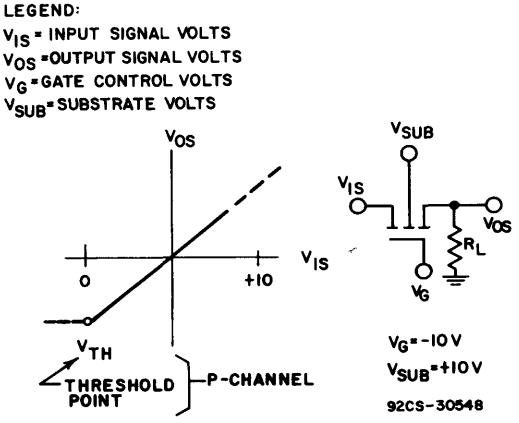


Fig. 12 – Switch characteristics of a single p-channel MOS transistor.

COS/MOS transmission-gate characteristics in Fig. 13.

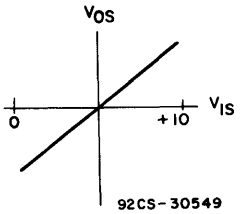


Fig. 13 – Composite switch characteristics of a COS/MOS transmission gate.

CD4016 Switch

The RCA COS/MOS CD4016 is a quad bilateral switch, or transmission gate. Each of the four independent transmission gates requires only a single control signal (an inverter is built in for each control line); i.e., both the p-channel and n-channel devices in a given switch are biased on or off simultaneously by the control signal. A functional diagram for the CD4016 is shown in Fig. 14. The schematic diagram for one of the four identical stages is given in Fig. 15.

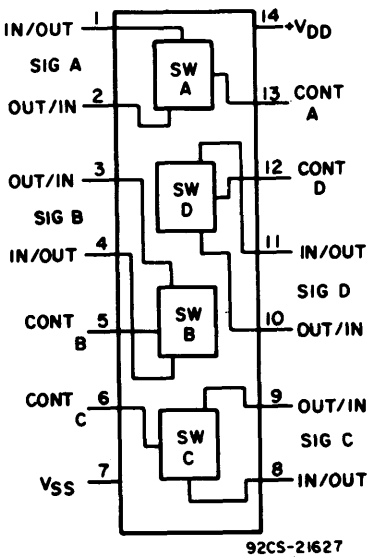


Fig. 14 – Functional diagram for the CD4016 quad bilateral switch.

The CD4016 quad bilateral switch can be used to perform the four common switch

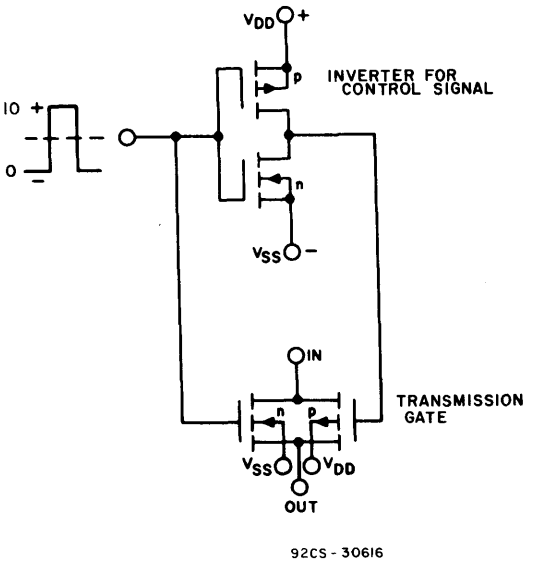


Fig. 15 – Schematic diagram for one of the four identical stages of the CD4016 quad bilateral switch.

functions (i.e., SPST, SPDT, DPST, and DPDT), as shown in Fig. 16.

Three-State Logic (Common Busing)

Transmission gates and analog multiplexer/demultiplexer circuits are extremely useful in coupling and decoupling from a common bus line. Either high or low signals can be placed on the bus line; with both gates off, the transmission gate presents a very high impedance to the line. (More information on busing is given in Chapter XI **Microprocessors and Memory Interfacing.**)

FLIP-FLOPS

Three basic types of flip-flops can be configured in COS/MOS: R-S (Set-Reset), D-type (Master-Slave), and the J-K flip-flop.

Set-Reset Flip-Flops

Two NOR gates may be connected as shown in Fig. 17 to form a set-reset flip-flop. When the set and reset inputs are low, one output is low and the other high, and there is a stable condition. If a positive pulse is applied to the

set input, its associated n-channel device is turned on; the $\overline{Q}$ output then goes low and the Q output goes high. After the pulse period both inputs are again low, and the flip-flop is in another stable condition.

Applying a positive pulse to the reset input causes the Q output to go low and the $\overline{Q}$ output to go high; after the pulse period both inputs are again low and the flip-flop is in the original stable condition. Additional positive pulses on the same input do not cause any change in the output, i.e., the pulses must be applied alternately to the inputs to change the condition of the flip-flop.

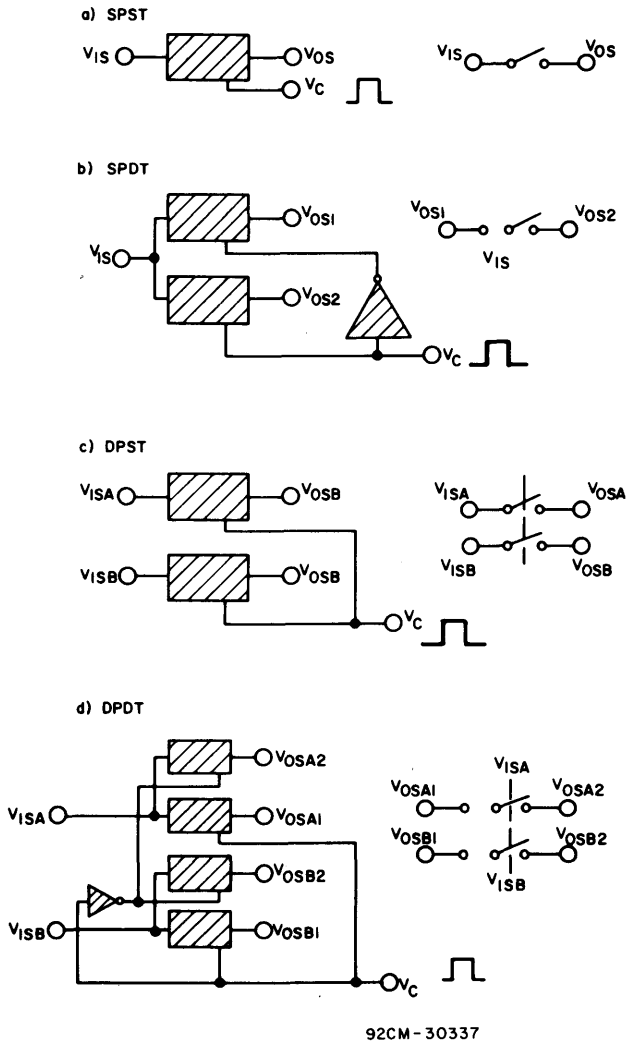
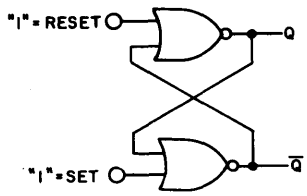


Fig. 16 – Basic switch functions using the CD4016 quad bilateral switch. a) Single-pole single-throw, b) Single-pole double throw, c) Double-pole single-throw, and d) Double-pole double-throw.



TRUTH TABLE

S	R	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$	NO CHANGE
1	0	1	0	
0	1	0	1	
1	1	0	0	

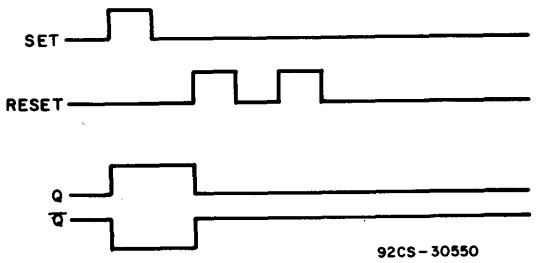
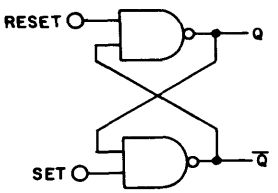


Fig. 17 – Logic diagram, truth table, and associated pulse shapes for a set-reset flip-flop using NOR gates.

Two NAND gates may also be used to form a set-reset flip-flop, as shown in Fig. 18. In this configuration, negative-going pulses are used to switch the outputs.



TRUTH TABLE

S	R	Q	$\overline{Q}$	
0	1	0	1	
1	0	1	0	
1	1	Q	$\overline{Q}$	NO CHANGE
0	0	1	1	

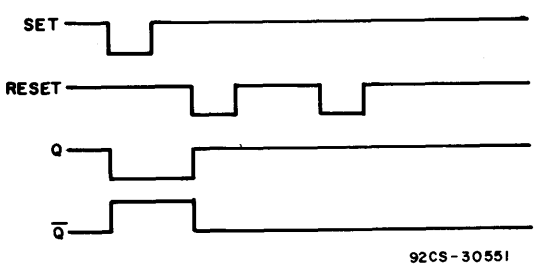


Fig. 18 – Logic diagram, truth table, and associated pulse shapes for a set-reset flip-flop using NAND gates.

D Flip-Flops

Fig. 19 shows the circuit for a D-type (Master-Slave) flip-flop. The block diagram shows a master flip-flop formed from two inverters and two transmission gates (shown as switches) that feed a slave flip-flop having a similar configuration. The transmission-gate control signal is called the "clock" because it controls the timing of the operations. When the clock is at a low level, the TG1 transmission gates are closed and the TG2 gates are open. This configuration allows the master flip-flop to sample incoming data, while the slave holds the data from the previous input and feeds it to the

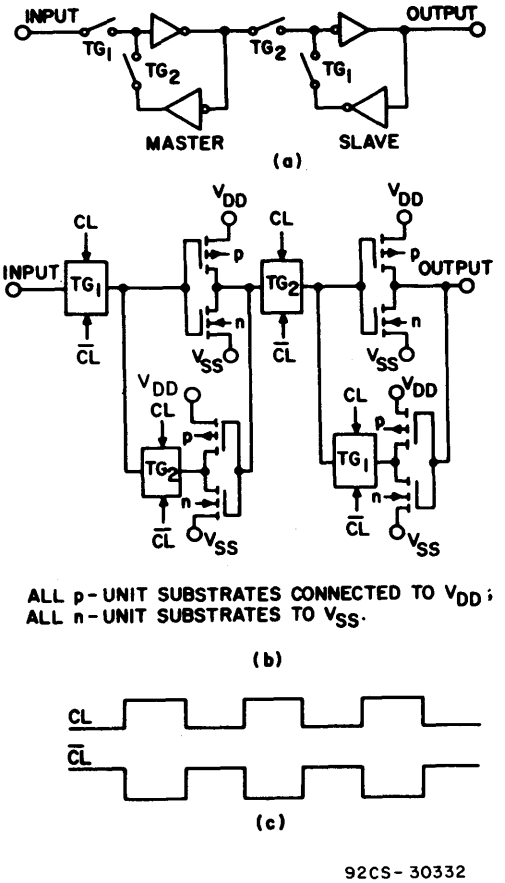


Fig. 19 – Logic diagram, simplified schematic, and clock-pulse diagrams for a D-type flip-flop.

output. When the clock is high, the TG1 transmission gates open and the TG2 gates close, so that the data is held in the master and fed to the slave.

The D-type flip-flop is static and holds its state indefinitely if no clock pulses are applied, i.e., it stores the state of the input prior to the last clocked input pulse. As shown in Fig. 19, both the clock (CL) and the inverted clock ($\overline{CL}$) are required to control the transmission gates; clock inversion is accomplished by an inverter.

Set and reset capability are added to the D-type flip-flop by changing the inverters in the master and slave sections to NOR gates. Fig. 20 shows the logic diagram and truth table for a D-type flip-flop with set and reset capability. As shown in the truth table, a high on the reset input sets the Q output low; a high on the set input forces the Q output high.

The RCA-CD4013 consists of two identical independent D-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs, and Q and $\overline{Q}$ outputs, as shown in Fig. 21. The logic level present at the data (D) input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is accomplished by a high level on the set or reset line, respectively. (If the set or reset inputs are not used, they must be tied low so the gate does not float.)

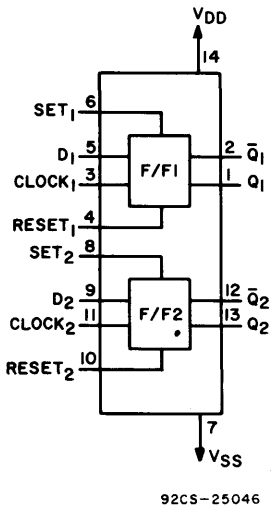
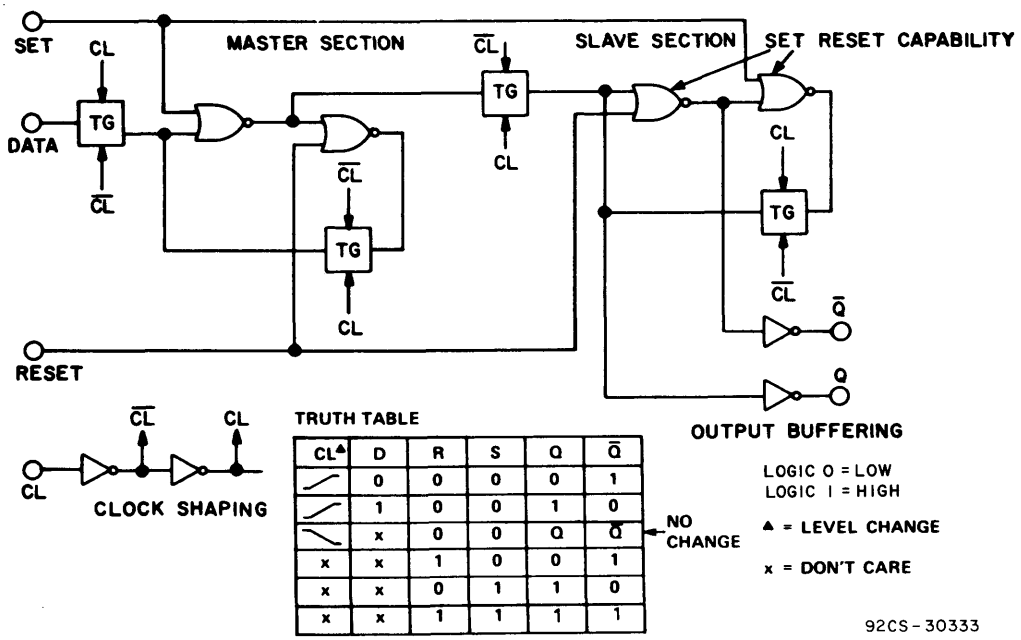


Fig. 21 – Functional diagram for CD4013 dual D flip-flop with set-reset capability.

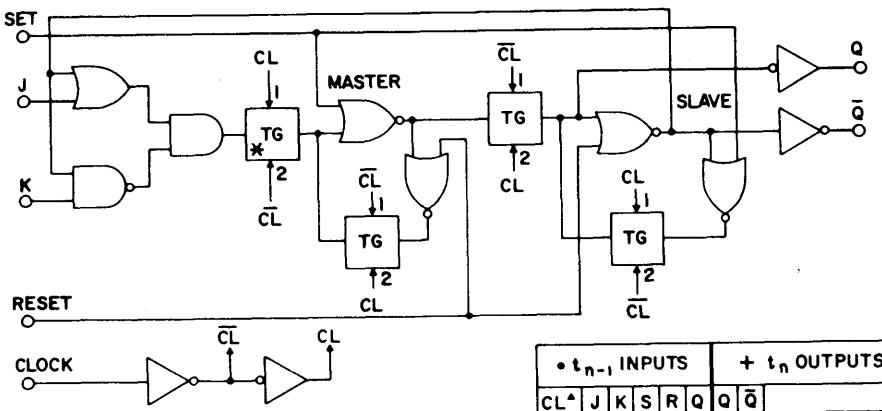
J-K Flip-Flops

The logic diagram and truth table for a J-K flip-flop are shown in Fig. 22. The J-K flip-flop is similar to the D-type flip-flop, but has some additional circuitry to accommodate



CL▲	D	R	S	Q	$\overline{Q}$
↗	0	0	0	0	1
↗	1	0	0	1	0
↘	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

Fig. 20 – Logic diagram and truth table for a D-type flip-flop with set-reset capability.



• t_{n-1} INPUTS						+ t_n OUTPUTS		
CL▲	J	K	S	R	Q	Q	$\bar{Q}$	
⌐	1	X	0	0	0	1	0	
⌐	X	0	0	0	1	1	0	
⌐	0	X	0	0	0	0	1	
⌐	X	1	0	0	1	0	1	
¬	X	X	0	0	X			←(NO CHANGE)
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	*	*	

▲ – LEVEL CHANGE
X – DON'T CARE
* – INVALID CONDITION
• – t_{n-1} REFERS TO THE TIME INTERVAL PRIOR TO THE POSITIVE CLOCK PULSE TRANSITION.

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Fig. 22 – Logic diagram and truth table for a J-K flip-flop.

the J and K inputs. The J and K inputs provide separate clocked set and reset inputs, and allow the flip-flop to change state on successive clock pulses (this capability is known as the "toggle mode"). The J-K flip-flop circuit also has set and reset capability; the inverters in the master and slave flip-flop each have an added OR input for direct (unclocked) setting or resetting of the flip-flop.

The RCA-CD4027 is a single monolithic integrated circuit containing two identical independent J-K master-slave flip-flops, as shown in Fig. 23. Each flip-flop has provisions for individual J,K, set, reset, and clock input signals; buffered Q and $\bar{Q}$ signals are provided as outputs.

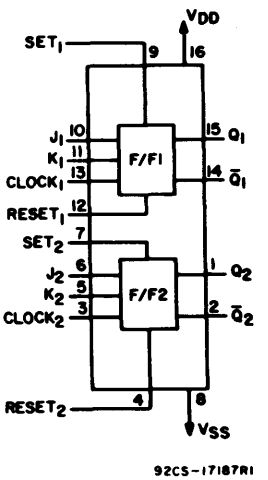

Fig. 23 – Functional diagram for CD4027 dual J-K flip-flop with set-reset capability.

SHIFT REGISTERS

Shift registers are basically flip-flops (usually D-type) connected so that the Q output of each stage becomes the D input of the following stage. The clock is common so that all shifting occurs synchronously.

Static Shift Registers

Fig. 24 shows a block diagram for a basic multi-stage static shift register and illustrates the associated pulse shapes. RCA provides a variety of static shift registers ranging from four stages (CD4015) to 64 stages (CD4031). (Additional information is given in Chapter VIII Shift Registers and Counters.)

Dynamic Shift Registers

Fig. 25 shows the circuit diagram and clock-pulse diagram for a two-stage dynamic shift register; each stage consists of two inverters and two transmission gates. Each transmission gate is driven by two out-of-phase clock signals arranged so that when alternate transmission gates are turned on, the others are turned off. The shift register uses the input capacitance of the inverters for temporary storage of the signals. When the first transmission gate in each stage is turned on, it couples the signal from the previous stage to the inverter. When the transmission gate is turned off on the next half-cycle of the clock, the signal is stored on the input capacitance to the inverter. The signal remains at the output of the inverter, where it is available to the next transmission gate, which is then turned on. Again, this signal is applied to the input of the next inverter where it is stored in the input capacitance of the inverter, making the signal available at the output of the stage. Thus, a signal progresses to the right by one-half stage on each half-cycle of the clock, or by one stage per clock cycle.

Because dynamic shift registers depend on stored charge, which is subject to slow decay, there is a minimum frequency at which they will operate; reliable operation can be expected at frequencies as low as 5 kHz.

The RCA-CD4062 is a 200-bit dynamic shift register with recirculating capability, useful as a long serial memory or time-delay circuit. This circuit is described in Chapter VIII Shift Registers and Counters.

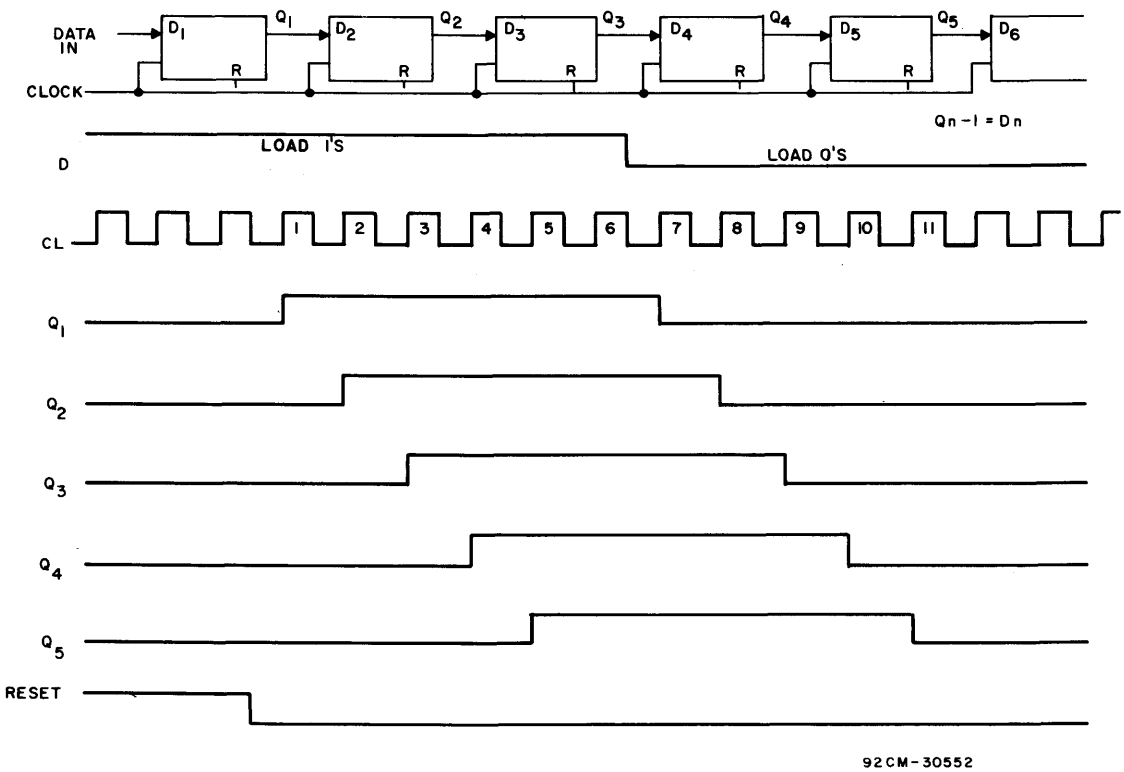

Fig. 24 – Block diagram and pulse shapes for a multi-stage static shift register.

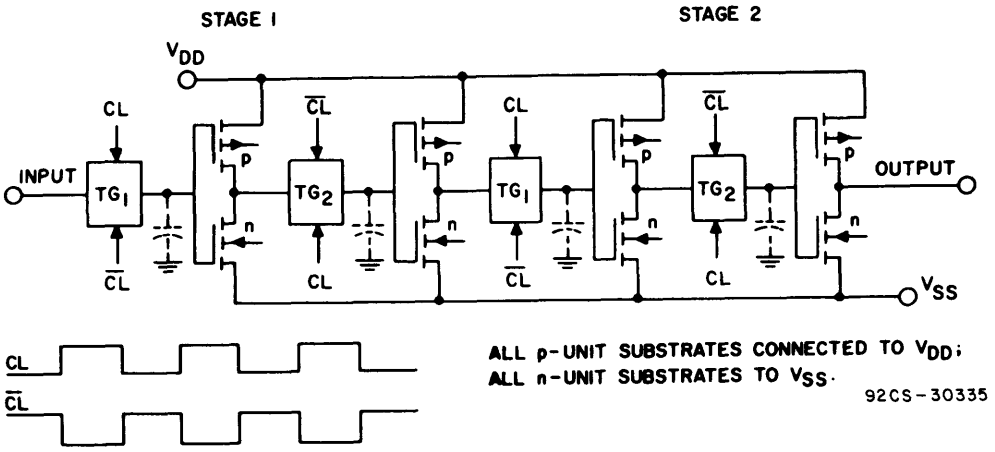

Fig. 25 — Circuit diagram and pulse shapes for a two-stage dynamic shift register.

COUNTERS

Binary (divide-by-two per stage) counters are similar to shift registers except that the D input to each stage is connected to the $\overline{Q}$ output of the stage. The Q and $\overline{Q}$ outputs of one stage become the Clock and $\overline{Clock}$ inputs of the following stage. Fig. 26 shows the logic diagram, block diagram, and associated pulse shapes for a five-stage binary counter.

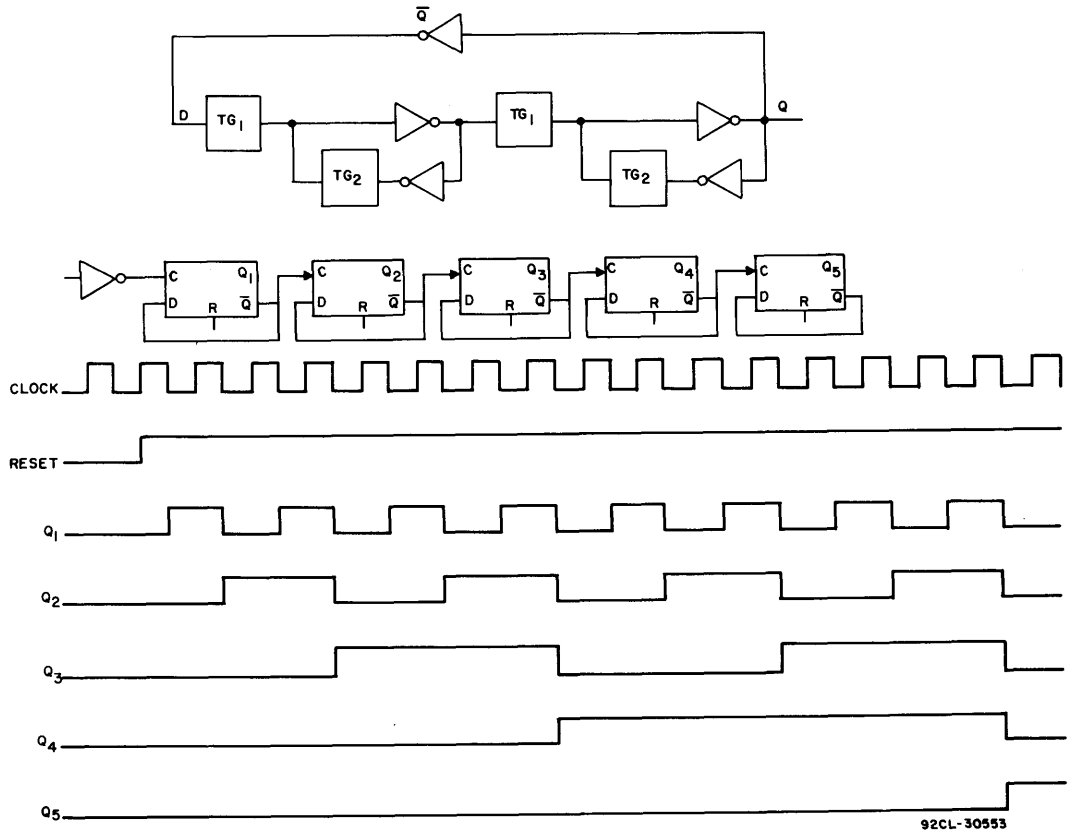

Fig. 26 — Logic diagram, block diagram, and pulse shapes for a five-stage binary counter.

The counter is advanced one count on the negative-going transition of each input pulse.

RCA provides a variety of binary counters ranging from seven stages (CD4024) to 21 stages (CD4045). These circuits are described in Chapter VIII Shift Registers and Counters.

MEMORY CELLS

The basic storage element common to most RCA COS/MOS memories consists of two COS/MOS inverters cross-coupled to form a flip-flop, as shown in Fig. 27. Single-transistor transmission gates are used as a simple and efficient means of performing the logic functions associated with storage-cell selection (i.e., the sensing and storing operations).

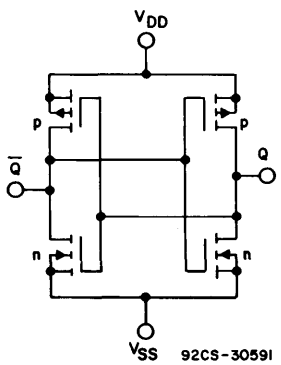

Fig. 27 – Basic storage element of COS/MOS memories.

The resulting word-organized storage cell, shown in Fig. 28, is composed of six transistors, a word line W, and two digit-sense lines D1 and D2. Addressing is accomplished by energizing a word line; this action turns on

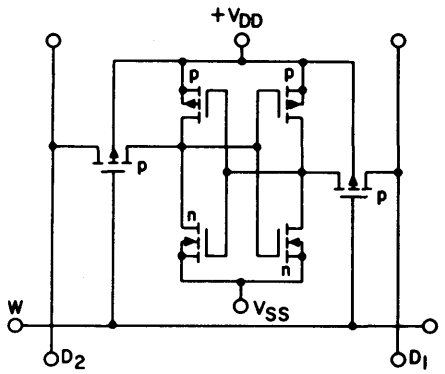

Fig. 28 – A word-organized storage cell (W is the word line; D1 and D2 are data lines).

the p-channel devices on both sides of the selected cell. (Because the cell in Fig. 28 uses p-channel devices, a ground-level voltage is required for selection.)

Fig. 29 shows an eight-transistor bit-organized memory cell that uses X-Y selection. Large memory arrays use a modification of this circuit in which the Y-select transistors are common for each column of storage elements.

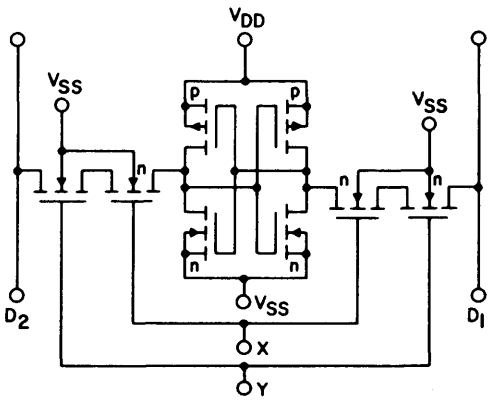

Fig. 29 – Eight-transistor bit-organized memory cell with X-Y selection.

III. Characteristics of RCA COS/MOS Devices

RCA COS/MOS digital integrated circuits are specified in two voltage-supply ranges: A-series types operate from 3 to 15 volts, and B-series types operate from 3 to 20 volts.

FEATURES OF COS/MOS B-SERIES TYPES

As compared to A-series types, COS/MOS B-series types are characterized by higher output-drive-current capability, balanced outputs (symmetrical p-channel and n-channel characteristics), and improved static protection circuitry. RCA B-series types meet or exceed all the requirements of the JEDEC Tentative Standard "Standard Specifications for B-Series CMOS Devices".

The JEDEC Standard establishes the use of a suffix "UB" for CMOS products that meet all the B-series specifications except that the logical outputs of the devices are not buffered and the input low voltage (V_{IL}) and input high voltage (V_{IH}) specifications are 20 percent and 80 percent of the supply voltage, V_{DD}, respectively. The "B" suffix defines only buffered-output devices in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

RCA supplies both buffered (B) and unbuffered (UB) versions of the popular NOR and NAND gates to make the advantages of both available to designers. Table II briefly compares the features of the two versions. (For additional information, refer to RCA Application Note ICAN-6558, "Understanding Buffered and Unbuffered CMOS Characteristics".)

A-SERIES CHARACTERISTICS

Static electrical characteristics for RCA A-series COS/MOS digital integrated circuits are given in Table III.

B-SERIES CHARACTERISTICS

Static electrical characteristics for RCA B-series COS/MOS digital integrated circuits

Table II – Comparison of Features of Buffered (B) and Unbuffered (UB) Versions of NOR and NAND Gates

Characteristic	Buffered Version ("B")	Unbuffered Version ("UB")
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Low
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

Table III – Static Electrical Characteristics for "A"-Series COS/MOS Digital Integrated Circuits (Full Package-Temperature Range)

SYMBOL	PARAMETER	CONDITIONS				LIMITS			UNITS
		V_{IN} (V)	V_O (V)		V_{DD} (V)				
			Min.	Max.		Min.	Typ.	Max.	
V_{OL}	Output Low Voltage	5 10	– –	– –	5 10	– –	0 0	0.05 0.05	V
V_{OH}	Output High Voltage	0 0	– –	– –	5 10	4.95 9.95	5 10	– –	V
V_{NL} (SSI Types)	Noise Voltage (Input Low)	– –	3.6 7.2	– –	5 10	1.5 3	2.25 4.5	– –	V
V_{NH} (SSI Types)	Noise Voltage (Input High)	– –	– –	1.4 2.8	5 10	1.5 3	2.25 4.5	– –	V
V_{NL} (MSI Types)	Noise Voltage (Input Low)	– –	4.2 9	– –	5 10	1.5 3	2.25 4.5	– –	V
V_{NH} (MSI Types)	Noise Voltage (Input High)	– –	– –	0.8 1	5 10	1.5 3	2.25 4.5	– –	V
V_{NML}	Noise Margin (Input Low)	– –	4.5 9	– –	5 10	1 1	– –	– –	V
V_{NMH}	Noise Margin (Input High)	– –	– –	0.5 1	5 10	1 1	– –	– –	V
I_{IL}, I_{IH}	Input Leakage Low	–	–	–	15	–	$\pm 10^{-5}$	±1	μA
I_L	Quiescent Device Leakage	–	–	–	5,10,15	See Data Sheets			μA
I_{DN}, I_{DP}	Output Source and Sink Current	–	–	–	5,10	See Data Sheets			mA

NOTE: Logic Level Inversion Assumed.

are given in Table IV. Table V shows the B-series types included in each of three categories of device complexity: (1) gates and inverters; (2) buffers, flip-flops, latches and multi-level gates (MSI-1 types); and (3) complex logic (MSI-2 types).

Table VI lists the standard definitions for many of the specified ac parameters for COS/MOS devices. The figures associated with Table VI show the parameter waveforms and test requirements. Figs. 30 through 45 show curves of device characteristics and include data on transition time, propagation delay time, and output drive current as a function of supply voltage.

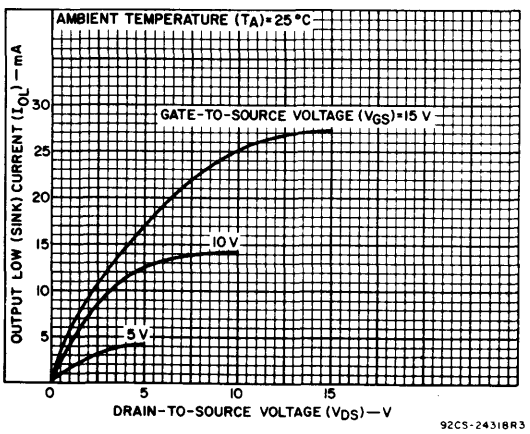

Fig. 30 – Typical output n-channel drain characteristics for COS/MOS B-series types.

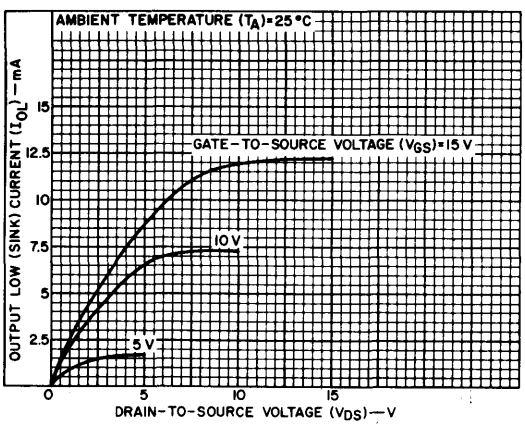

Fig. 31 – Minimum output n-channel drain characteristics for COS/MOS B-series types.

Table IV – Static Electrical Characteristics for "B"-Series COS/MOS Digital Integrated Circuits (Full Package-Temperature Range)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,F,H Packages Values at -40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max. Gates, Inverters	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Buffers, Flip-Flops, Latches, Multi-Level Gates (MSI-1 Types)		0,5	5	1	1	30	30	–	0.02	1	
		0,10	10	2	2	60	60	–	0.02	2	
		0,15	15	4	4	120	120	–	0.02	4	
		0,20	20	20	20	600	600	–	0.04	20	
Complex Logic (MSI-2 Types)		0,5	5	5	5	150	150	–	0.04	5	
		0,10	10	10	10	300	300	–	0.04	10	
		0,15	15	20	20	600	600	–	0.04	20	
		0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max. B Types	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5, 13.5	–	15	4				–	–	4	
UB Types	0.5, 4.5	–	5	1				–	–	1	
	1, 9	–	10	2				–	–	2	
	1.5, 13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min. B Types	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5, 13.5	–	15	11				11	–	–	
UB Types	0.5, 4.5	–	5	4				4	–	–	
	1, 9	–	10	8				8	–	–	
	1.5, 13.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0, 18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

Table V — Classification According to Circuit Complexity

Gates/ Inverters

CD4000B
CD4000UB
CD4001B
CD4001UB
CD4002B
CD4002UB
CD4007UB
CD4011B
CD4011UB
CD4012B
CD4012UB
CD4016B■
CD4023B
CD4023UB
CD4025B
CD4025UB
CD4048B
CD4066B
CD4068B
CD4069UB
CD4071B
CD4072B
CD4073B
CD4075B
CD4078B
CD4081B
CD4082B

Buffers/Flip-Flop/ Latches/Multi-Level Gates (MSI-1)

CD4009UB■
CD4010B■
CD4013B
CD4019B
CD4027B
CD4030B
CD4041UB
CD4042B
CD4043B
CD4044B
CD4047B
CD4049UB■
CD4050B■
CD4070B
CD4077B
CD4085B
CD4086B
CD4093B
CD4095B
CD4096B
CD4098B
CD4502B
CD40106B
CD40107B■
CD40109B
CD40174B
CD40257B

Complex Logic (MSI-2)

CD4006B
CD4008B
CD4014B
CD4015B
CD4017B
CD4018B
CD4020B
CD4021B
CD4022B
CD4024B
CD4026B
CD4028B
CD4029B
CD4031B
CD4032B
CD4033B
CD4034B
CD4035B
CD4038B
CD4040B
CD4045B
CD4046B■
CD4051B■
CD4052B■
CD4053B■
CD4054B■
CD4055B■
CD4056B■
CD4060B
CD4063B
CD4067B■
CD4076B
CD4089B
CD4094B
CD4097B■
CD4099B
CD4508B
CD4510B
CD4511B■
CD4512B
CD4514B
CD4515B
CD4516B
CD4517B
CD4518B
CD4520B
CD4527B
CD4532B
CD4536B
CD4555B
CD4556B
CD4585B
CD4724B
CD40100B
CD40101B
CD40102B
CD40103B
CD40104B
CD40105B
CD40108B
CD40110B
CD40114B
CD40147B
CD40160B
CD40161B
CD40162B
CD40163B
CD40181B
CD40182B
CD40192B
CD40193B
CD40194B
CD40208B

■Indicates types for which, because of special design requirements, one or more static characteristics differ from the standardized data.

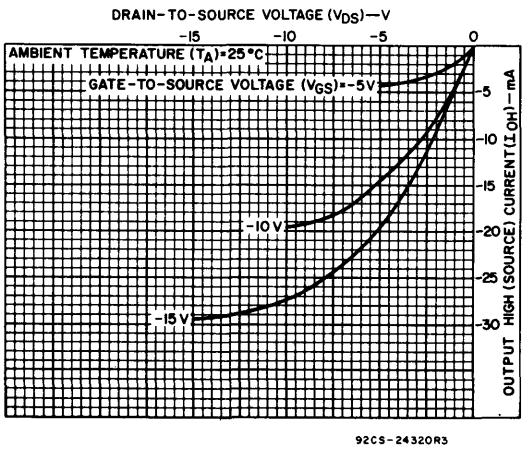

Fig. 32 — Typical output p-channel drain characteristics for COS/MOS B-series types.

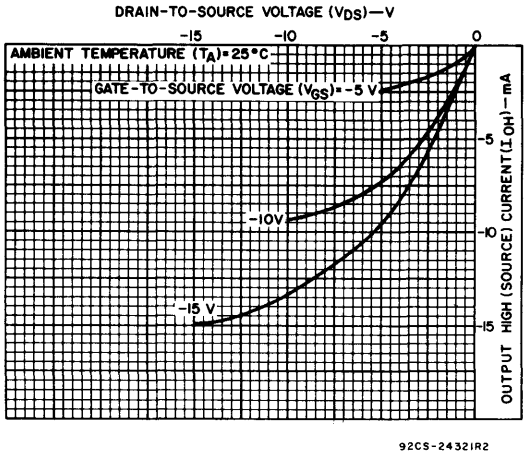

Fig. 33 — Minimum output p-channel drain characteristics for COS/MOS B-series types.

Table VI – Dynamic Electrical Characteristics – Definitions

Characteristic	Symbol	Limits Max.	Limits Min.	Notes (Fig.)
Propagation Delay:				
Outputs going high to low	t_{PHL}	X		(A)
Outputs going low to high	t_{PLH}	X		
Output Transition Time:				
Outputs going high to low	t_{THL}	X		(A)
Outputs going low to high	t_{TLH}	X		
Pulse Width-Set, Reset, Preset Enable, Disable, Strobe, Clock	t_{WL} or t_{WH}		X	1 (B)
Clock Input Frequency	f_{CL}	X		1,2 (B)
Clock Input Rise and Fall Time	t_{rCL}, t_{fCL}	X		(B)
Set-Up Time	t_{SU}		X	1 (C)
Hold Time	t_H		X	1 (C)
Removal Time - Set, Reset, Preset-Enable	t_{REM}		X	1 (C)
Three-State Disable Delay Times:				
High level to high impedance	t_{PHZ}	X		(D)
High impedance to low level	t_{PZL}	X		(D)
Low level to high impedance	t_{PLZ}	X		(D)
High impedance to high level	t_{PZH}	X		(D)

NOTE: (1) By placing a defining min. or max. in front of definition, the limits can change from min. to max., or vice versa.

(2) Clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

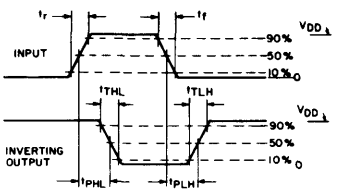

Fig. A – Transition times and propagation delay times, combination logic.

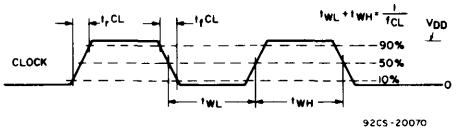

Fig. B – Clock-pulse rise and fall times and pulse width.

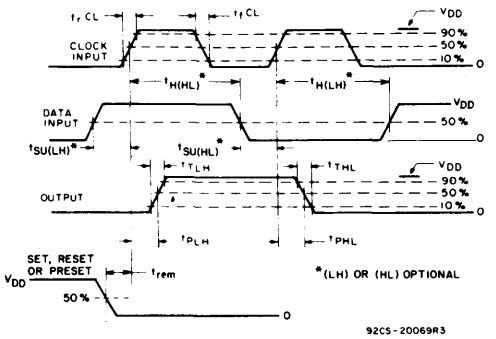

Fig. C – Setup times, hold times, removal time, and propagation delay times for positive-edge triggered sequential logic circuits.

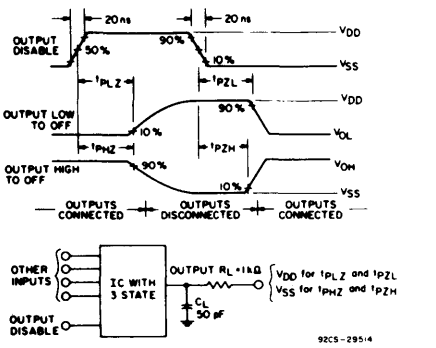

Fig. D – Three-state propagation delay wave shapes and test circuit.

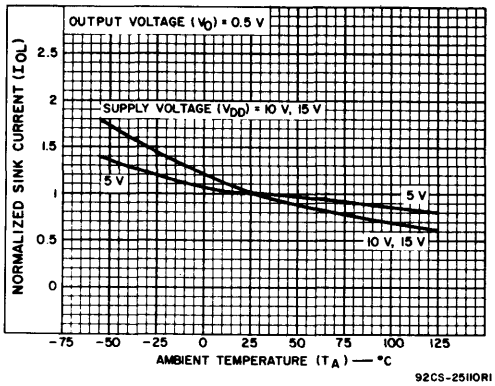

Fig. 34 — Variation of normalized sink current (I_{OL}) with temperature for COS/MOS B-series types.

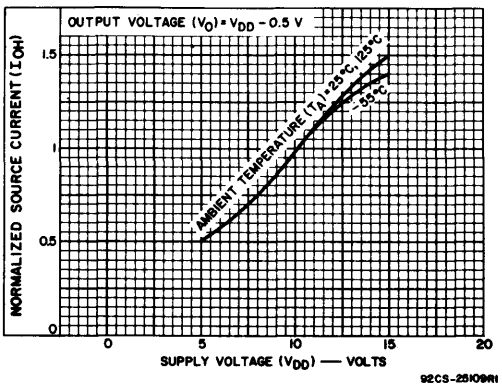

Fig. 37 — Variation of normalized source current (I_{OH}) with supply voltage for COS/MOS B-series types.

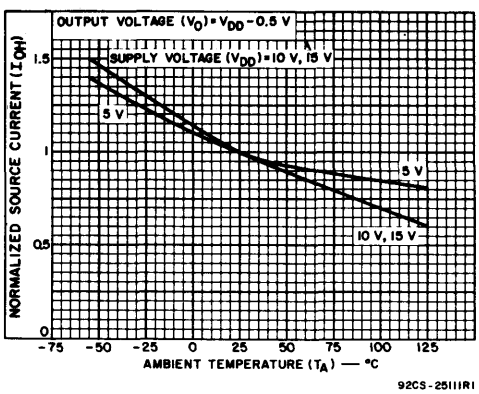

Fig. 35 — Variation of normalized source current (I_{OH}) with temperature for COS/MOS B-series types.

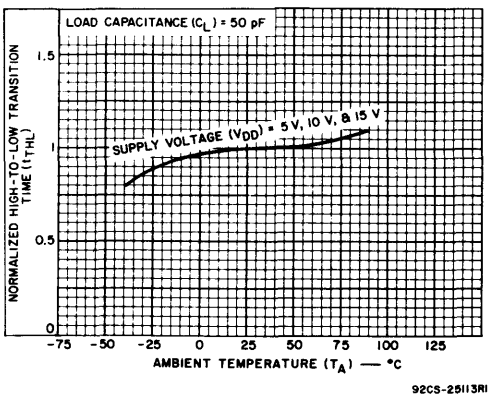

Fig. 38 — Variation of normalized high-to-low transition time (t_{THL}) with temperature for COS/MOS B-series types.

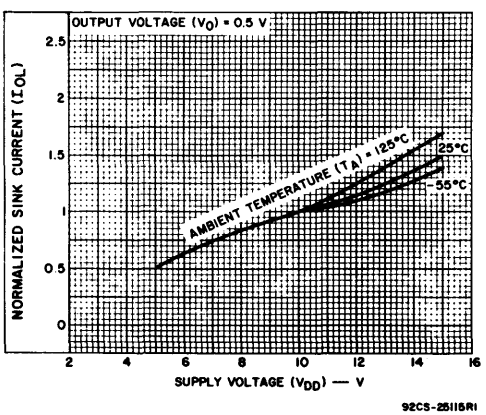

Fig. 36 — Variation of normalized sink current (I_{OL}) with supply voltage for COS/MOS B-series types.

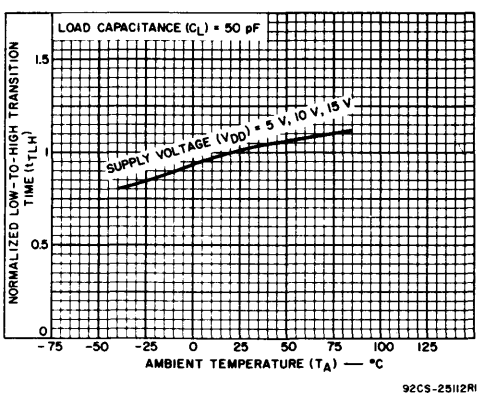

Fig. 39 — Variation of normalized low-to-high transition time (t_{TLH}) with temperature for COS/MOS B-series types.

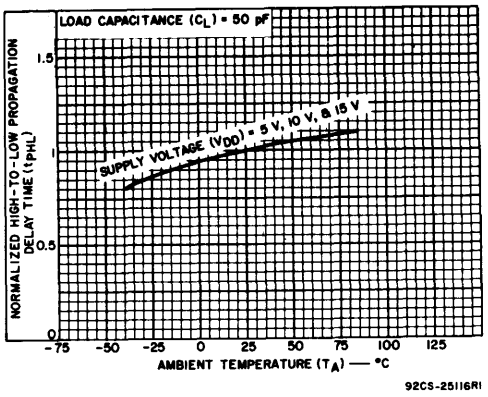

Fig. 40 — Variation of normalized high-to-low propagation delay time (t_{PHL}) with temperature for COS/MOS B-series types.

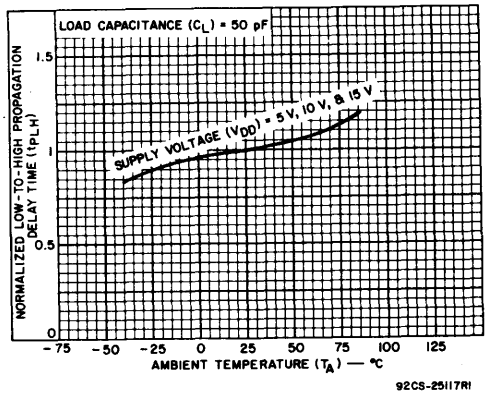

Fig. 41 — Variation of normalized low-to-high propagation delay time (t_{PLH}) with temperature for COS/MOS B-series types.

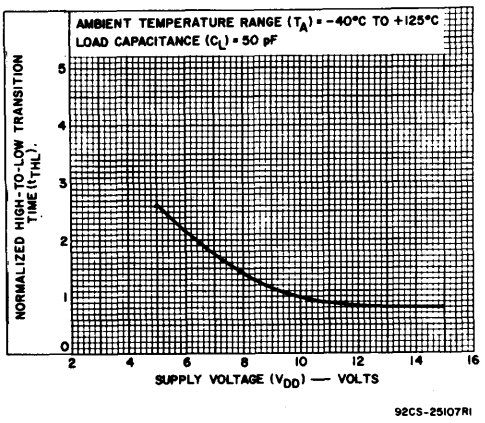

Fig. 42 — Variation of normalized high-to-low transition time (t_{THL}) with supply voltage for COS/MOS B-series types.

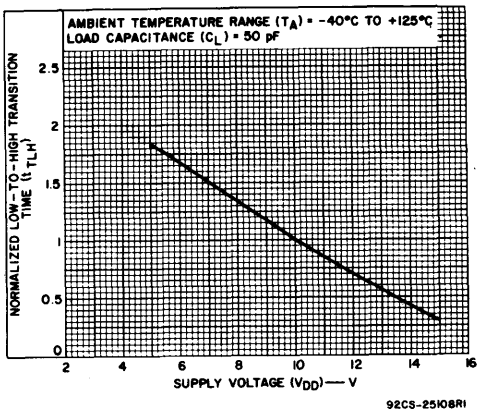

Fig. 43 — Variation of normalized low-to-high transition time (t_{TLH}) with supply voltage for COS/MOS B-series types.

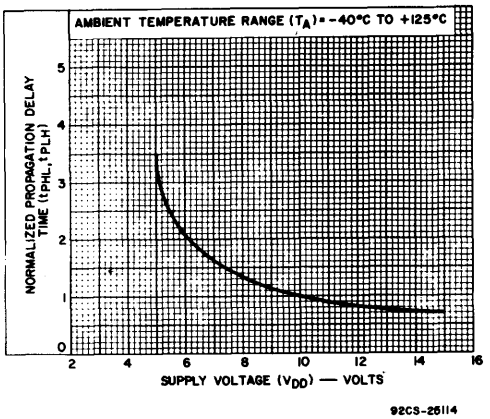

Fig. 44 — Variation of normalized propagation delay time (t_{PHL}, t_{PLH}) with supply voltage for COS/MOS B-series types.

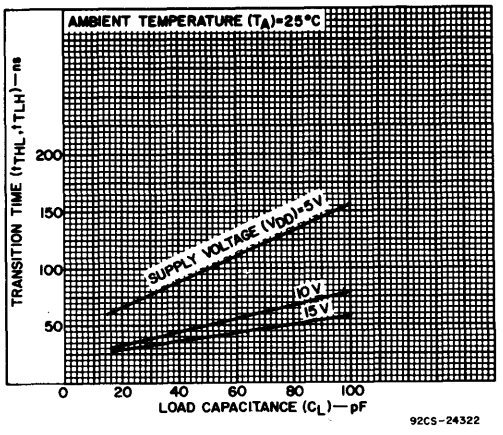

Fig. 45 — Variation of normalized transition time (t_{THL}, t_{TLH}) with load capacitance at three levels of supply voltage for COS/MOS B-series types.

PACKAGES

Maximum ratings for power dissipation and the operating temperature range depend on package type. RCA COS/MOS integrated circuits are available in four types of packages:

Dual-in-line welded-seal or brazed-seal ceramic ..... D suffix
Dual-in-line frit-seal ceramic ..... F suffix
Dual-in-line plastic ..... E suffix
Ceramic flat pack (MIL types only) . K suffix

Depending on the requirements of the individual integrated-circuit type, the number of leads may range from 8 to 40 per package.

For bonding on hybrid substrates, unpackaged die (chips) are also available; they are indicated by an H suffix.

MAXIMUM RATINGS AND RECOMMENDED OPERATING CONDITIONS

The maximum ratings for both A- and B-series COS/MOS digital integrated circuits are given in Table VII. Ratings which differ because of the package type used are indicated. Table VIII gives the recommended operating conditions for A- and B-series types.

TYPES CLASSIFIED BY FUNCTION

The RCA COS/MOS digital integrated circuit types are classified by function in Table IX. The Table includes A, B, and UB types. Types suitable for more than one of the functions listed are indicated by footnote symbols which cross-refer the type to the additional functional category.

Table VII – Maximum Ratings for "A"- and "B"-Series Types
(Absolute-Maximum Values)

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal):
STANDARD "A"-SERIES TYPES ..... –0.5 to +15 V
HIGH-VOLTAGE "B"-SERIES TYPES ..... –0.5 to +20 V
INPUT VOLTAGE,RANGE, ALL INPUTS ..... –0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ("B"-series only) ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D,F) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

Table VIII – Recommended Operating Conditions for the "A"- and "B"-Series Types

Characteristic		Limits Min.	Max.	Units
Supply-voltage range (For T_A = Full package-temperature range)	"A" series	3	12	volts
	"B" series	3	18	volts

Table IX – RCA COS/MOS Digital Integrated Circuit Types Classified by Function

GATES

Single-Level

NOR/NAND		OR/AND	Buffers & Inverters
CD4000B	CD4012B	CD4071B	CD4007UB
CD4000UB	CD4012UB	CD4072B	CD4007A
CD4000A	CD4012A	CD4073B	CD4009UB
CD4001B	CD4023B	CD4075B	CD4009A
CD4001UB	CD4023UB	CD4081B	CD4010B
CD4001A	CD4023A	CD4082B	CD4010A
CD4002B	CD4025B		CD4041UB
CD4002UB	CD4025UB		CD4041A
CD4002A	CD4025A		CD4049UB
CD4011B	CD4068B		CD4049A
CD4011UB	CD4078B		CD4050B
CD4011A	CD40107B		CD4050A
			CD4069UB
			CD4502B
			CD40107B

Multi-Level

Multi-function/AOI	Decoders/ Encoders	Schmitt Trigger
CD4019B	CD4028B	CD4093B
CD4019A	CD4028A	CD40106B
CD4030B	CD4514B	
CD4030A	CD4515B	
CD4037A	CD4532B	
CD4048B	CD4555B*	
CD4048A	CD4556B*	
CD4070B■	CD40147B	
CD4077B■		
CD4085B		
CD4086B		

■See Comparators

*See Demultiplexers

MULTIVIBRATORS

Flip-Flops/Latches

CD4013B	CD4096B
CD4013A	CD4099B**
CD4027B	CD4508B
CD4027A	CD4724B**
CD4042B	CD40174B
CD4042A	Astable/ Mono-stable
CD4043B	
CD4043A	
CD4044B	
CD4044A	CD4047B
CD4076B**	CD4047A
CD4095B	CD4098B

**See Storage Registers

REGISTERS

Shift	Storage	FIFO Buffer
CD4006B	CD4076B	CD40105B
CD4006A	CD4099B	
CD4014B	CD4724B	
CD4014A	CD40108B●	
CD4015B	CD40208B●	
CD4015A		
CD4021B		
CD4021A		
CD4031B		
CD4031A		
CD4034B		
CD4034A		
CD4035B		
CD4035A		
CD4062A		
CD4094B		
CD4517B		
CD40100B		

●See Multiport Register

COUNTERS

Binary Ripple	Synchronous
CD4020B	CD4017B
CD4020A	CD4017A
CD4024B	CD4018B
CD4024A	CD4018A
CD4040B	CD4022B
CD4040A	CD4022A
CD4060B	CD4029B
CD4060A	CD4029A
	CD4059A
	CD4510B
	CD4516B
TIMERS	CD4518B
	CD4520B
CD4045B	CD40102B
CD4045A	CD40103B
CD4536B	CD40160B
	CD40161B
	CD40162B
	CD40163B
	CD40192B
	CD40193B

MULTIPLEXERS/ DEMULTIPLEXERS

Analog/Digital Data Selectors

CD4016B▲	
CD4016A▲	
CD4019B	
CD4019A	
CD4051B	
CD4052B	
CD4053B	
CD4066B▲	
CD4066A▲	
CD4067B	
CD4097B	
CD4555B⊕	
CD4556B⊕	
CD40257B	

▲See Quad Bilateral Switch

⊕See Decoders/ Encoders

PHASE-LOCKED LOOP

CD4046B
CD4046A

QUAD BILATERAL SWITCHES

CD4016B◆
CD4016A◆
CD4066B◆
CD4066A◆

◆See Multiplexers

INTER-FACE CIRCUITS

CD4009UB
CD4009A
CD4010B
CD4010A
CD4049UB
CD4049A
CD4050B
CD4050A
CD40107B
CD40109B
CD40115

ARITHMETIC CIRCUITS

Adders/ Comparators	ALU/Rate Multipliers	Parity Generator/ Checker	Multiport Register
CD4008B	CD4057A	CD40101B	CD40108B*
CD4008A	CD4089B		CD40208B*
CD4030B	CD4527B		
CD4030A	CD40181B		
CD4032B	CD40182B		
CD4032A			
CD4038B			
CD4038A			
CD4063B			
CD4070B♦			
CD4077B♦	♦See Multifunc-tion/AOI		*See Storage Register
CD4585B			

DISPLAY DRIVERS

With Counter	For LCD* Drive	For LED●● Drive
CD4026B	CD4054B	CD4511B
CD4026A	CD4055B	
CD4033B	CD4056B	
CD4033A		
CD40110B		

*Liquid-Crystal Display

●●Light Emitting Diode

CROSS-POINT SWITCHES

CD22100▼
CD22101▼
CD22102▼

MEMORY

CD40114B

▼Indicates types designed for special applications. Ratings and characteristics data for these types differ in some aspects from the standardized data for A- and B-series types.

EXTRA-VALUE AND MIL TYPES

For sensitive applications requiring devices of extra quality, the RCA COS/MOS Extra-Value Program offers dual-in-line package types with certain special screening and testing. The processing of these types includes a 168-hour burn-in at 125°C at a 12-volt bias to substantially reduce early failures ("infant mortality"). As a result of the processing and testing added to the comprehensive controls and tests carried out on standard product, AQL's of 0.25 percent parametric and 0.15 percent functional are achieved.

For critical applications, RCA offers a line of COS/MOS devices processed and screened in accordance with MIL-STD-883 and MIL-M-38510.

IV. Handling and Operating Considerations

HANDLING COS/MOS DEVICES

The silicon dioxide layer located immediately over the channel and beneath the gate electrode creates the very high input impedance of MOS devices (greater than 10^{12} ohms). For best device operation, this channel oxide must be extremely thin, i.e., in the order of 1000 angstroms. As a result, it is susceptible to damage by high static electric charges which can accumulate on the surfaces of the devices and on personnel handling them. Unlike semiconductor junction p-n diodes, which can sustain breakdown a number of times without permanent damage, the MOS gate can be shorted by a single voltage excursion to the oxide breakdown point of about 80 volts.

To protect the oxide layer, COS/MOS devices are shipped in either anti-static or conductive carriers. The same technique or other means of minimizing the potential difference between leads should be maintained. Units should be stored in the RCA carriers or with their pins imbedded in conductive foam. The following procedures should be followed during handling, inspection, and test:

1. Use conductive work surfaces.
2. Ground all handling equipment. (Alternatively, ionized-air blowers can reduce charge build-up in areas where grounding is not feasible.)
3. Require personnel handling units to wear a conductive wrist strap grounded through a 1-megohm resistor.
4. Place units in conductive or anti-static carriers when they are moved from one work station to another.

BUILT-IN PROTECTION NETWORKS

Each COS/MOS device has a built-in protection network. Fig. 46 shows the original protection network incorporated in all CD4000A-series and some CD4000B-series devices. This network can protect the

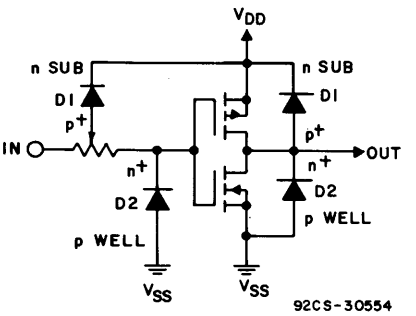

Fig. 46 – Protection network used in all CD4000A-series and some CD4000B-series devices.

gate oxide against electrostatic discharges up to 1 kilovolt. The diode D1 is a distributed resistor-diode network that is made up of p+-to-n-substrate material and has a voltage breakdown in the range of 30 to 50 volts. Diode D2 is a separate diode that is built of n+-to-p-well material and has a breakdown in the range of 30 to 40 volts.

Fig. 47 shows an improved protection network used on new RCA COS/MOS devices which increases the typical gate-oxide protection to 4 kilovolts. The improvement in protection can be attributed to several different phenomena. The addition of a resistor and distributed diode in the output path

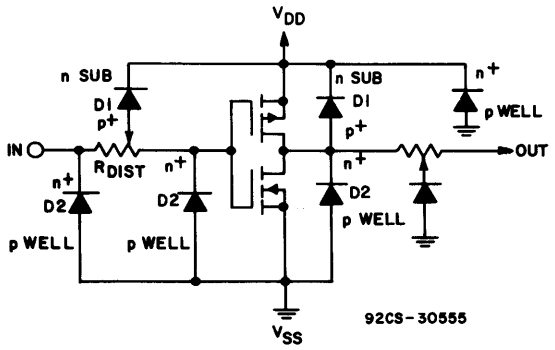

Fig. 47 – Improved protection network used on new RCA COS/MOS devices.

provides diode clamping of transient signals as well as an RC filtering effect which is crucial at the instant any transient is impressed upon the device. In addition, the extra diode at the input allows the input to be clamped whenever V_{IN} is equal to or less than 0.7 V more negative then V_{SS}.

Probably the most important improvement is due to the inclusion of a well-defined zener diode from V_{DD} to V_{SS}. There are 12 separate modes in which a COS/MOS device may receive an electrostatic discharge, as shown in Fig. 48. When the device is not connected to a supply voltage, protection for many of these modes is guaranteed only by the reverse breakdown capability of the diode from V_{DD} to V_{SS}. In the improved protection circuit this diode has a well-defined breakdown voltage of approximately 25 volts, low "on" resistance, and on-chip ground and V_{DD} distribution that are as low impedance as feasible.

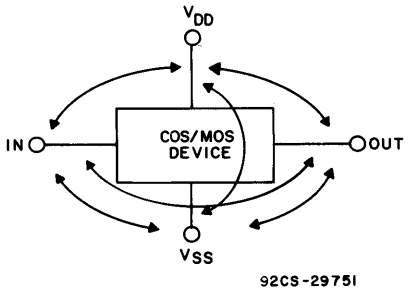

Fig. 48 – Electrostatic discharge modes.

OPERATING PRECAUTIONS

Latch-up Considerations

During operation near the maximum ratings, care should be taken to suppress any transients and to avoid any large capacitive loads. Excursions above maximum ratings can force CMOS devices into a p-n-p-n SCR "latch-up" mechanism which can be destructive.

"Latch-up" is defined as the creation of a low-resistance path between the power supply and ground by an electrical pulse which remains a low-resistance path after the pulse. There are several parasitic bipolar transistors in CMOS circuits. Fig. 49 shows how the p-n-p lateral transistor and an n-p-n vertical transistor are formed. These parasitic transistors form the equivalent SCR structure shown in Fig. 50. The conditions necessary for SCR turn-on are as follows:

1. The beta of the n-p-n vertical transistor times the beta of the p-n-p lateral transistor must be equal to or greater then unity ($\beta_{\text{n-p-n}} \times \beta_{\text{p-n-p}} \geq 1$).

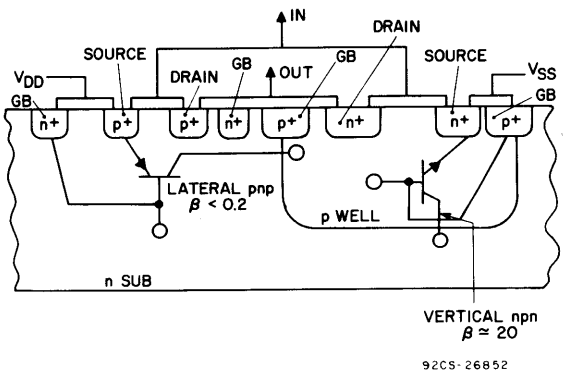

Fig. 49 – Parasitic bipolar transistors in CMOS circuits.

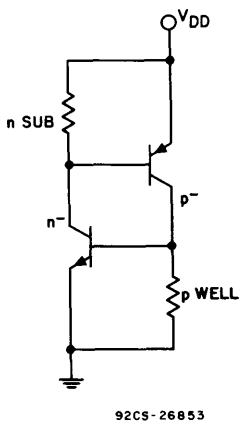

Fig. 50 – Equivalent circuit for the SCR structure present in CMOS circuits.

2. The lateral p-n-p and vertical n-p-n base-emitter junctions must be forward-biased, usually initiated by high transient currents in the n substrate (see Fig. 50).

3. The bias circuit which applied power to V_{DD} and to the input must be capable of supplying current equal to the holding current of potential SCR's.

Fig. 51 shows a curve of I_{DD} as a function of V_{DD} which illustrates the effect of secondary breakdown and SCR latch-up. Table X shows typical values of breakdown voltage and sustaining voltage and current for COS/MOS A-series and B-series devices.

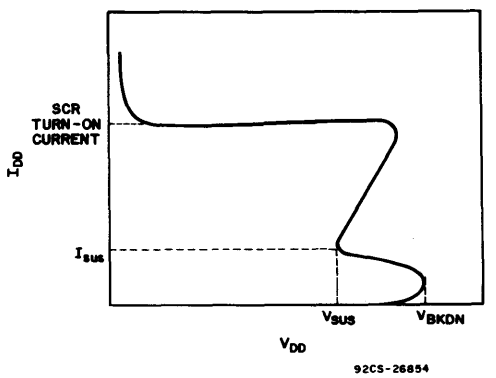

Fig. 51 – Curve illustrating effect of secondary breakdown and SCR latch-up.

Table X – Typical Breakdown Values for A- and B-Series Devices

	A Series	B Series
Breakdown Voltage (V)	17	25
Sustaining Voltage (V)	15	22
Sustaining Current (mA)	2 to 40 (type-dependent)	50 to 100

These values show that B-series devices are harder to latch than A-series types because of their higher breakdown voltage.

Operating-Rule Summary

Observation of the following operating rules will enhance reliable operation of any CMOS system:

1. When a low-impedance pulse generator or separate power supply is used for the device inputs, the main device power supply should always be turned on before the independent signal sources are turned on. When a system is being shut down, the independent signal sources should be turned off before the main power supply is turned off. (In other words, $V_{SS} \leqslant V_I \leqslant V_{DD}$). This rule will avoid input-diode damage.

2. In the case of CD4009 and CD4010, the diode between V_{CC} (pin 1) and V_{DD} (pin 16) should not be forward-biased. V_{DD} should always be greater than V_{CC}. This rule is especially important during power sequencing.

3. When series resistors are used on power supplies, it is wise to avoid biasing inputs to the non-limited side of the supply. This action will eliminate the potential hazard of forward-biasing the input diodes.

4. The power-supply polarity should not be reversed, i.e., $V_{DD} - V_{SS} > -0.5$ V. Such reversal could overdissipate the substrate diode.

5. All inputs should be terminated. A floating input can force the CMOS

inverter into a linear mode and cause faulty operation as a result of the large current.

6. When CMOS devices are interfaced in PC cards, a pull-up or pull-down resistor should always be used if there is a possibility of an input becoming open.

7. CMOS outputs should not be connected in the "wire-OR" configuration. Instead, 3-state outputs or transmission gates hould be used.

8. Output loads should not be returned to voltages greater than V_{DD} or less than V_{SS}; otherwise, the output diodes will be turned on.

VOLTAGE AND DISSIPATION CONSIDERATIONS

Recommended Maximum Operating Voltage

RCA COS/MOS digital integrated circuits have maximum ratings of 15 volts for A-series types and 20 volts for B-series types. However, because logic systems can experience transient conditions on the power-supply line which, when added to the nominal power-bus voltage, could exceed the safe limits of circuits connected to the power bus, the recommended operating supply-voltage ranges are 3 to 12 volts for A-series types and 3 to 18 volts for B-series types. (The 3-volt minimum limit is set by the sum of the threshold of the p-channel and n-channel transistors.)

Power Dissipation

Total power dissipation in a COS/MOS device is the sum of the static (or quiescent) dissipation and the dynamic (or ac) dissipation.

Quiescent dissipation, which is due to leakage effects, is much smaller than dynamic dissipation, varying from a few nanowatts to a few microwatts depending upon the complexity of the circuit.

Dynamic dissipation is comprised of two elements: "through" current that exists during the transition from one logic level to another, when both p-channel and n-channel devices are momentarily conducting, and the power-supply current required to charge node and output capacitances during switching. "Through" current is usually only about 10 percent of the charging current, particularly for systems which have fast rise and fall times. Dynamic dissipation P_{dyn} can be expressed as follows:

$$P_{dyn} = C \times V_{DD}^2 \times f$$

Because dynamic power dissipation is a function of the supply voltage squared, the system designer seeking to minimize power consumption should specify the lowest possible operating voltage.

NOISE IMMUNITY AND NOISE MARGIN

AC noise is usually considered to comprise noise spikes with pulse widths shorter than the propagation delay of a logic gate; dc noise spikes are considered to have pulse widths longer than the propagation delay of one gate. AC noise immunity, which varies in direct proportion to dc noise immunity, is largely a function of the propagation delays and output transition times of logic gates and, therefore, is a function of input and output capacitances.

The high dc noise immunity of COS/MOS integrated circuits is a result of the complementary structure of the inverter (common to all COS/MOS devices), which has a near-ideal input-output transfer characteristic. The switching point is typically midway (45 to 50 per cent) between the "0" and "1" output logic levels. Fig. 52 shows the steep transfer characteristic exhibited during transitions.

The noise-immunity voltage (V_{IL} or V_{IH}) is that noise voltage at any one input that does not propagate through the system. Minimum noise immunity for buffered B-series COS/MOS devices is 30, 30, and 27 per cent, respectively, for supply voltages of 5, 10, and 15 volts; for all unbuffered gates, it

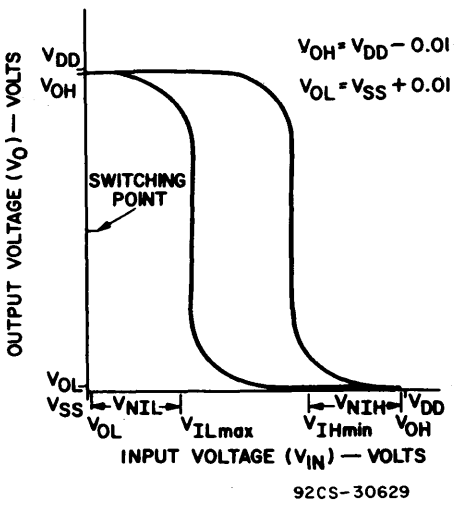

Fig. 52 – Typical inverter transfer characteristic.

is 20 per cent of V_{DD}. The V_{IL} and V_{IH} specifications define the maximum permissible additive noise voltage at an input terminal when input signals are at the supply rails.

Noise margin is the difference between the noise-immunity voltage (V_{IL} or V_{IH}) and the output voltage V_O. Noise-margin voltage is the maximum voltage that can be impressed upon an input voltage V_{IN} (where V_{IN} is the output voltage of the preceding stage) at any or all logic I/O terminals without upsetting the logic or causing any output to exceed the noise-immunity ratings. Noise margins for buffered B-series COS/MOS devices are 1, 2, and 2.5 volts, respectively, for supply voltages of 5, 10, and 15 volts.

Because noise immunity is proportional to supply voltage, designers aware of noise in the system environment should specify a high enough operating voltage to guarantee immunity. The excellent noise immunity of COS/MOS devices reduces the need for highly regulated and filtered power supplies, as compared to the requirements of other logic families.

VOLTAGE LOGIC-LEVEL DEFINITIONS

The voltage logic-level terms used in the published data for COS/MOS digital devices are defined below and illustrated in Fig. 53.

V_{OL} is the maximum output at low level with no noise at the input. For an inverter, V_{OL}(max) is the output level when the input is tied to V_{DD}, assuming only capacitive loading at the

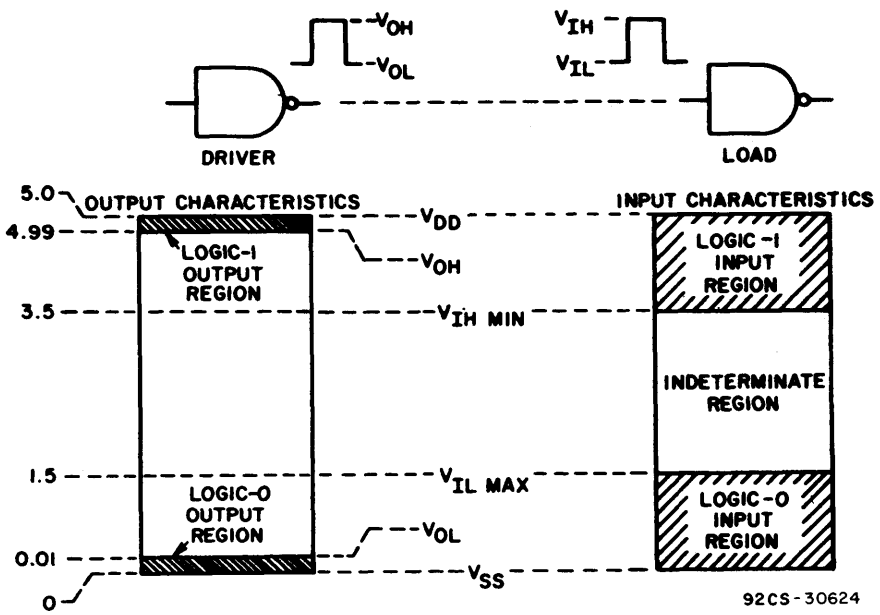

Fig. 53 – Output-to-input logic-level characteristics.

output. For COS/MOS circuits, $V_{OL} = V_{SS} - 0.05$ volts.

V_{OH} is the minimum output at high level with no noise at the input. For an inverter, V_{OH}(min) is the output level when the input is grounded, assuming only capacitive loading at the output. For COS/MOS circuits, $V_{OH} = V_{DD} - 0.05$ volt.

V_{IL}(max) is the maximum input at low level for which the output logic level does not change state.

V_{IH}(min) is the minimum input at high level for which the output does not change state.

INPUT CONSIDERATIONS

Unused Inputs

Floating inputs are not permitted with COS/MOS devices. Because the high-input-impedance COS/MOS gates might rise to a potential that would turn on both p-channel and n-channel devices, floating inputs result in logic malfunction and can also cause excessive power dissipation. All unused inputs must be tied to either $+V_{DD}$ or $-V_{SS}$; for gates, however, unused inputs may be tied to other used inputs.

Input Signal Swing

For optimum performance, input levels should be at full V_{DD} and V_{SS}. Because of the high dc noise immunity of COS/MOS devices, however, an input level from 70 per V_{SS} to 30 per cent of V_{DD} are acceptable. Fig. 54 shows the range of switching transfer characteristics for a COS/MOS integrated circuit for a supply voltage of 10 volts ($V_{DD} - V_{SS}$). The absolute maximum permissible swing at COS/MOS device inputs is from V_{SS} -0.5 volts to V_{DD} + 0.5 volts.

Paralleling Gate Inputs

The inputs of multi-input NAND or NOR gates are sometimes wired together and connected to a common source, as shown in Fig. 55. In the case of NAND gates such as

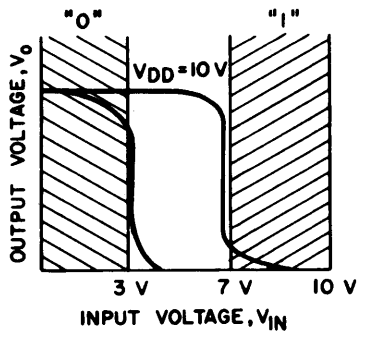

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Fig. 54 – Range of switching transfer characteristics.

the CD4012A, where as many as four input pins may be wired together, a slight increase in speed occurs when more than one input is tied to the same signal. In addition, the output source current of the device is increased in direct proportion to the number of inputs wired together.

When the inputs of a NOR gate are tied together to a common input signal, the gate experiences a higher sink current and a slight increase in speed. The speed increase in both NAND and NOR gates results from the lower "on" resistance of the paralleled devices. The increase in speed is minimized by a compensating speed decrease caused by the added capacitance of the driving source combined with the capacitance internal to the device itself.

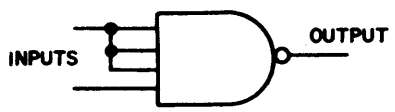

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Fig. 55 – Logic diagram of 4-input NAND gate with 3 inputs interconnected.

OUTPUT CONSIDERATIONS

Parallel Outputs and Inputs of Gates and Inverters

Both source and sink output current are increased when two or more similar devices on the same chip are paralleled as shown in Fig. 56. This increased drive capability also increases speed if the increase in capacitive

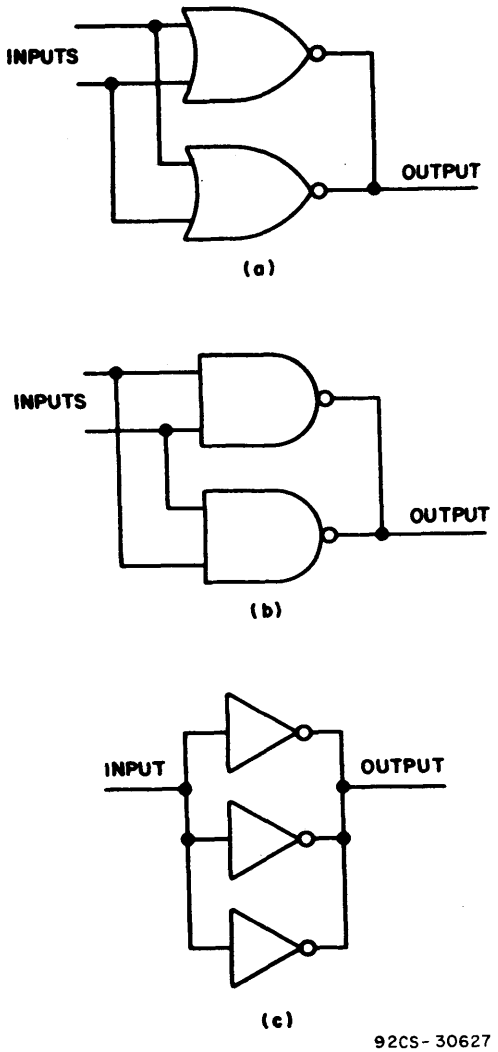


Fig. 56 – Typical device paralleling arrangements: (a) NOR gates, (b) NAND gates, (c) inverters.

loading is not excessive. When devices are parallel, power dissipation also increases. (Because of variations in threshold voltages between different chips, paralleling should be limited to devices on the same chip only.)

Capacitive Loading

CMOS logic systems should be designed to minimize capacitive loading. Capacitive loading decreases speed and increases power dissipation. In the design of a system, it should be realized that one COS/MOS unit load imposes a capacitance of 7.5 picofarads across the output of the COS/MOS circuit.

Wired-"OR" Function

In COS/MOS integrated circuits, common busing is not permitted at inverter outputs because of the complementary nature of the basic COS/MOS inverter circuit. With COS/MOS devices, therefore, the wired-OR function, which is sometimes referred to as the virtual-OR phantom-OR, is unrealizable using the outputs of active (gain-stage) inverters and gates. Fig. 57 shows the effect of

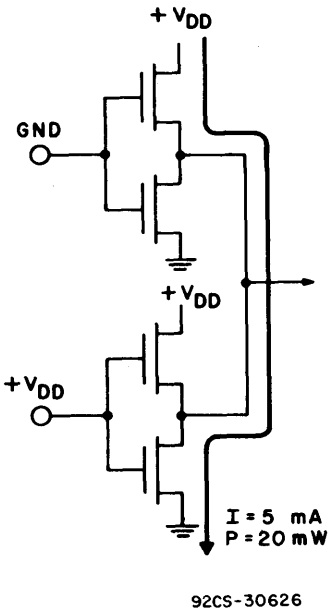


Fig. 57 – Effect of wired-OR connection on a basic COS/MOS inverter circuit. (This connection should be avoided.)

the wired-OR connection on a basic COS/MOS inverter circuit. Results equivalent to those provided by the wired-OR function are obtainable in COS/MOS logic by use of transmission gates and/or functional logic.

POWER-SUPPLY CONSIDERATIONS

Regulation and Filtering

COS/MOS devices switch reliably and operate with high noise immunity over a wide range of power-supply voltages (3 to 15 volts for A-series types, 3 to 20 volts for B-series types). As a result, an unregulated supply with minimal filtering may be used as long as

the maximum voltage limits are not exceeded and the minimum voltage (combination of lowest V_{DD} from unregulated supply and lowest peak of ripple) is sufficient for the required system speed. In other words, maximum system speed is dictated by the minimum power-source excursion. Information on switching speed as a function of supply voltage and load capacitance is given in the published data for COS/MOS integrated circuits.

Battery Operation

Because of their wide voltage range, COS/MOS logic circuits can be operated directly from inexpensive batteries which have a wide voltage excursion from beginning to end of life. The high noise immunity of COS/MOS devices provides another advantage in battery operation because the internal impedance of a battery is usually greater than that of most power supplies.

Zener-Diode-Reference Operation

Operation from zener-diode references not only protects COS/MOS devices from momentary line transients, but can also provide an effective power-supply source from dc sources which exceed maximum device voltage, such as a 28-volt aircraft supply. In the design of zener regulators such as that shown in Fig. 58, both the peak

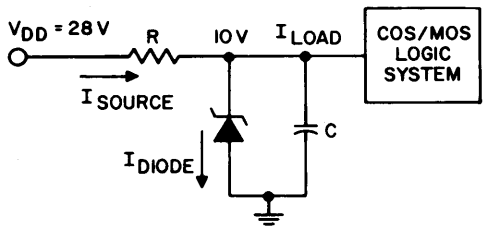


Fig. 58 – Zener regulator circuit.

switching currents and the rise and fall times of current must be considered in calculation of the R and C values.

CLOCK REQUIREMENTS

All sequentially operated static COS/MOS integrated circuits require a single-phase clock. The amplitude of the clock pulse should be equal to the single power-supply voltage V_{DD}. Fig. 59 shows the clock-edge

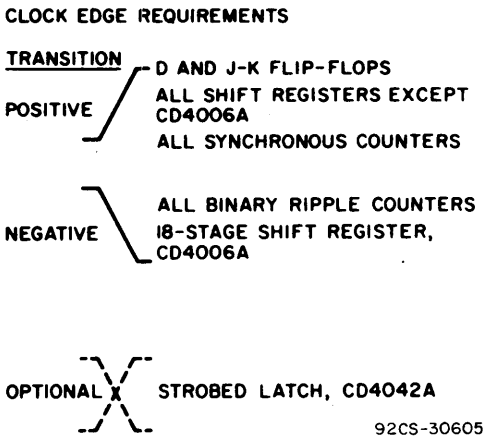


Fig. 59 – Clock-edge requirement for CD4000-series COS/MOS integrated circuits.

requirements for flip-flops, shift registers, counters, and latches included in the CD4000 series of COS/MOS integrated circuits.

Clock rise and fall times should not exceed 5 to 15 microseconds (depending on supply voltage) because of circuit design and possible cascading considerations. Minimum clock pulse width and maximum operating frequency are functions of the supply voltage and the type of device. Clock requirements for COS/MOS integrated circuits are given in the published data.

CASCADING CONSIDERATIONS

When sequential COS/MOS circuits such as flip-flops and shift registers are connected in cascade, the designer must take care that data are not lost in the transfer between different devices. Variations in the range of input switching levels and flip-flop time constants may result in a loss of data.

The input switching level of an active COS/MOS circuit has a 4-volt range (3 to 7 volts) for operation from a 10-volt supply, as shown earlier in Fig. 54. This range of switching levels is the result of the range of threshold variations inherent in present MOS technology. Although these variations present no problem in dc logic usage, they can affect error-free cascading of shift-register stages.

Fig. 60 shows an extreme example. In the circuit shown, stage Q1 triggers at a lower voltage level than stage Q2. With the slow clock rise time shown, the output of Q1 changes before any change occurs in Q2; the input to D of Q2, which should be high, has gone low before Q2 switches, and an error results in the output of Q2.

If two or more COS/MOS flip-flops (e.g., CD4013 or CD4027) or shift registers (e.g., CD4006 or CD4014) are cascaded, the clock rise time should be made less than the total of the fixed propagation delay plus the output transition time, as determined from the published data for the specific capacitive loading condition. For several shift-register device types such as in the CD4031, CD4094, or CD40107 this problem is avoided by the use of an internal delayed clock output or outputs clocked by CL.

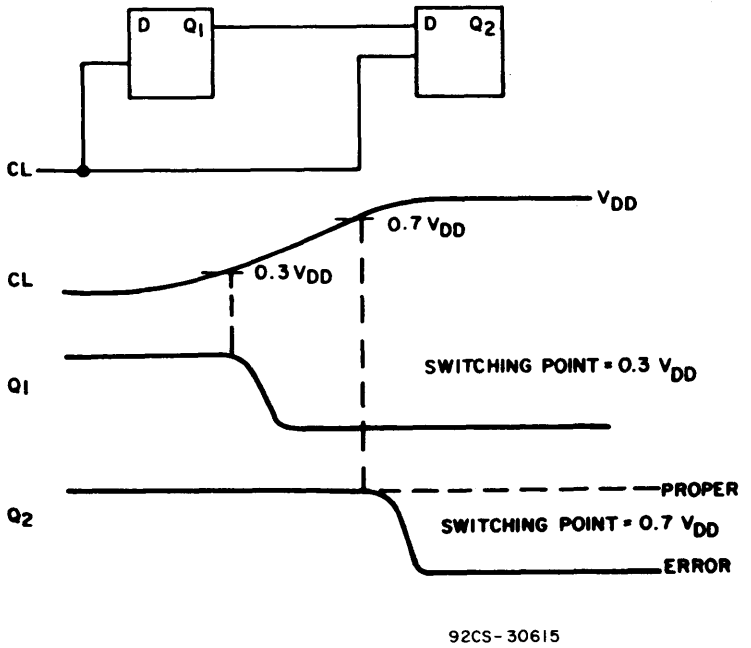


Fig. 60 – Error effect that results from a slow clock in cascaded circuits.

V. Interfacing COS/MOS

Proper interfacing between different logic families requires that the circuits selected operate at a common supply voltage and have logic-level compatibility. In addition, the devices must maintain safe power-dissipation levels and good noise immunity over the specified operating-temperature range. This chapter, after discussing the relationship between positive- logic and negative-logic systems, covers interfacing COS/MOS circuits with p-channel MOS, n-channel MOS, saturated bipolar logic (TTL, HNIL, DTL, and ECL) systems, and with discrete and electromechanical devices.

POSITIVE/NEGATIVE LOGIC CONVERSION

All published data and application information for COS/MOS circuits reference positive-logic functionality. The relationship between positive and negative logic can be explained with the aid of Table XI, a voltage truth table. In this table, H represents a high voltage and L a low voltage, X and Y represent inputs, and f(x,y) is the output. If the higher level, H, is assigned the value of logical 1, the circuit is said to operate under positive logic. If logical 1 is assigned to the lower level, L, the logic is negative.

Table XI – Voltage Truth Table

Inputs		Output
X	Y	f(x,y)
L	L	H
L	H	L
H	L	L
H	H	L

Possible Logic Assignments

Positive:	Negative:
H = logical 1	H = logical 0
L = logical 0	L = logical 1

Table XII – Logic Tables

Positive Logic L = 0, H = 1			Negative Logic L = 1, H = 0		
NOR Function			NAND Function		
X	Y	f(x,y)	X	Y	f(x,y)
0	0	1	1	1	0
0	1	0	1	0	1
1	0	0	0	1	1
1	1	0	0	0	1
f(x,y)	= X · Y		f(x,y)	= X + Y	
	= X + Y			= X · Y	

The positive and negative logic tables corresponding to the voltage truth table of Table XI are shown in Table XII. A positive-logic NOR gate and a negative-logic NAND gate represent two functions reversed in assignment. Therefore, a COS/MOS CD4001 quad two-input NOR gate used in a negative-logic system acts as a quad two-input NAND gate. A CD4011 quad two-input NAND gate acts as a quad two-input NOR gate in a negative-logic system.

The CD4024 is a seven-stage binary counter. In negative logic, the reset acts as a set and will set on a logical 0. Because the reset acts as a set, the output is all 1's instead of 0's, and the counter becomes a down-counter. Fig. 61 shows how some typical

COS/MOS circuit symbols are represented in positive and negative logic systems.

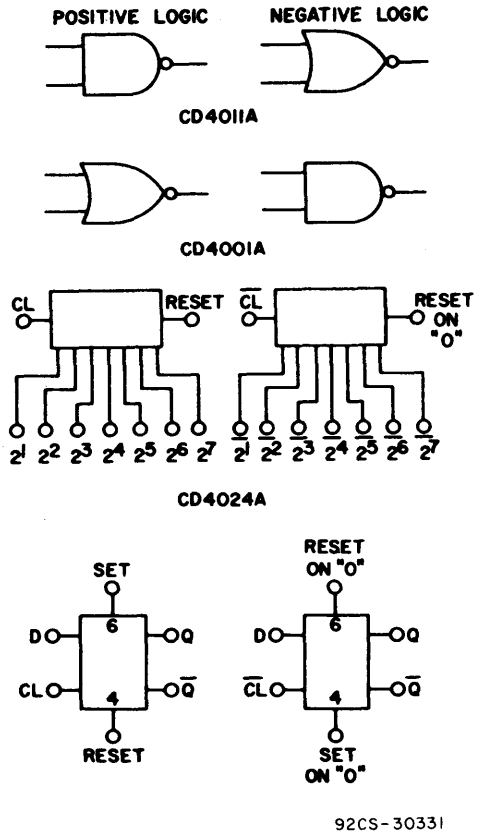


Fig. 61 — Common symbols for COS/MOS devices in positive- and negative-logic systems; symbols apply equally to all device types in a series.

INTERFACING WITH P-CHANNEL MOS

P-channel MOS systems utilize negative logic. P-channel MOS-transistor logic levels generally are -6 volts for low-threshold types and -15 volts for high-threshold types. Direct interface with COS/MOS logic circuits is achieved by operating the COS/MOS circuit at a V_{DD} of zero volts and a V_{SS} of either -6 or -15 volts, as required.

Silicon-gate PMOS static shift registers operating from 5-volt and -12-volt supplies are directly compatible with a COS/MOS system operating from the 5-volt supply with V_{SS} at zero volts. The only additional component required is a clamp diode to V_{SS} on the data output, as shown in Fig. 62, because the unloaded PMOS output voltage will go negative in the low output state.

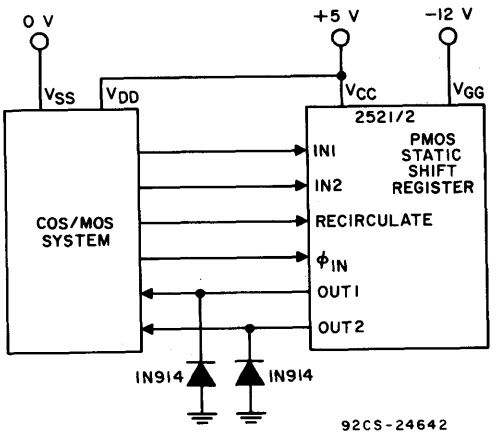


Fig. 62 — COS/MOS-to-PMOS static-shift-register interface.

INTERFACING WITH N-CHANNEL MOS

N-channel MOS-transistor logic levels are positive and within the voltage range of COS/MOS devices. Therefore, direct interface is possible.

The increasing use of n-channel MOS memories has brought about considerable interfacing between COS/MOS and NMOS circuits. In a system of 1-kilobit memories, such as the type 2102, which employ peripheral COS/MOS circuits for address, read/write, chip select, and data handling, the COS/MOS circuits can be supplied from the 5-volt power supply of the memory. Inputs to the memory are then COS/MOS-compatible, and direct interface is permitted. The data output requires only a single pull-up resistor, R_X, as shown in Fig. 63, to

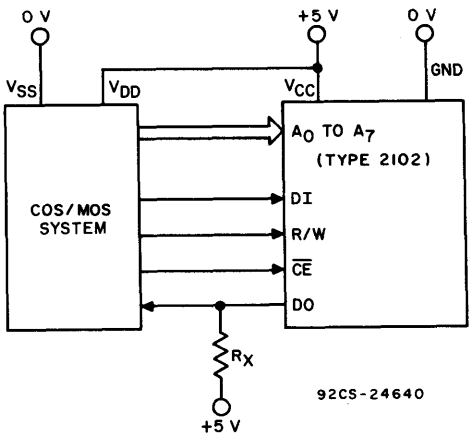


Fig. 63 — Direct interface between COS/MOS and a 1-kilobit memory, type 2102.

assure an acceptable high-state output voltage.

A 4-kilobit dynamic n-channel RAM, such as the 2107A, has 12-volt and -5-volt supplies as well as the 5-volt V_{CC} supply, as shown in Fig. 64. The COS/MOS peripheral circuitry

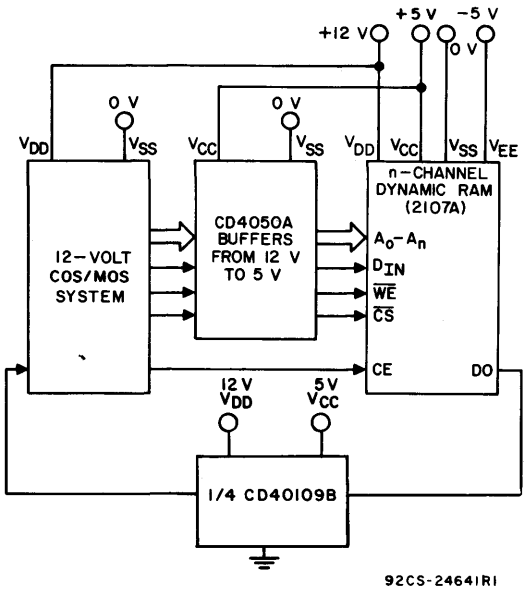


Fig. 64 – Interface from COS/MOS to an n-channel dynamic RAM.

this system is probably best operated from the 12-volt supply to assure good speed characteristics and noise immunity. The 5-volt input signals to the memory are provided by CD4050 buffers powered by the 5-volt V_{CC} supply. The 12-volt-swing chip-enable signal is directly compatible with the 12-volt COS/MOS system. The data output uses a single level shifter from a CD40109B to generate the required 12-volt logic swing; memories added to provide an increase in word capacity are wire-OR'ed at the data output pin of the memory.

(Further information on memory interfacing is given in Chapter XI, **Introduction to Microprocessors and Memory Interfacing.**)

Practically all recent developments in NMOS LSI technology are using the NMOS Depletion Load process. NMOS Depletion Load devices, unlike previous NMOS types, require only a single power supply with a voltage ranging from 5 to 7 volts. Direct interfacing of COS/MOS devices to NMOS Depletion Load inputs, therefore, can be accomplished. However, because of V_{OH} specification of approximately 50 per cent of V_{DD}, all NMOS Depletion Load device outputs require a pull-up resistor similar to that shown in Fig. 63.

INTERFACING WITH SATURATED BIPOLAR LOGIC

A need arises to interface COS/MOS logic with higher-speed, saturated bipolar logic when system logic speeds exceed 5 to 10 MHz. Optimum efficiency in system design is achieved by directly but alternately interfacing COS/MOS circuits and DTL or TTL circuits, i.e., taking full advantage of the superior COS/MOS logic characteristics at lower logic speeds and the high-speed capability of saturated bipolar logic where required.

COS/MOS and TTL

When TTL devices are interfaced with COS/MOS devices with a common power supply of 4.5 to 5.5 volts, the guaranteed active-pull-up TTL output voltage of 2.4 volts is lower than the minimum COS/MOS input voltage required to guarantee switching (3.5 volts), as shown in Fig. 65. This dif-

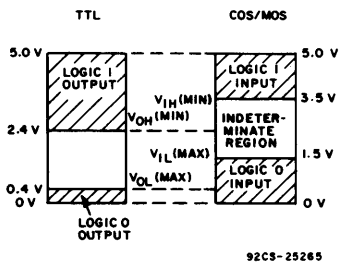


Fig. 65 – TTL-to-COS/MOS voltage levels.

ference is overcome by the use of an external resistor R_X, as shown in Fig. 66, which also serves as the resistor for open-collector-output TTL at a V_{DD} of 5 volts. The minimum value of R_X is fixed by the maximum sink current (e.g., 1.6 milliamperes for 74-series TTL and 36 milliamperes for 74LS-series TTL), and its maximum value is determined by I_{OH}, the "off"

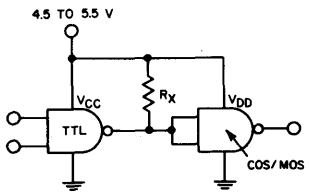


Fig. 66 – TTL-to-COS/MOS interface.

leakage of the output sink transistor. As shown in Table XIII, values of R_X between 1.5 and 4.7 kilohms are suitable for all the

Table XIII – Values of R_X for TTL-COS/MOS Interface

Characteristic	74	74H	74L	74LS	74S
R_X min. (ohms)	390	270	1.5k	820	270
R_X max. (kilohms)	4.7	4.7	27	12	4.7

TTL families under worst-case conditions. Because the COS/MOS input impedance is essentially capacitive, many COS/MOS inputs may be driven by a single TTL output; the actual number depends on the frequency of operation.

In the COS/MOS-to-TTL interface shown in Fig. 67, the requirement is to sink sufficient current in the low output state at a maximum output voltage of 0.4 volt. Table XIV shows the current-sinking capability of

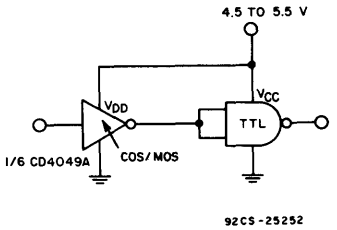


Fig. 67 – COS/MOS-to-TTL interface.

some CD4000-series devices. All B-series types have the same standard output drive and are capable of sinking one low-power Schottky load, worst case (0.36 milliampere at $V_{OUT} = 0.4$ V and $V_{DD} = 5$ V). For higher-power TTL types, the CD4049 and CD4050 buffers may be used. Table XV shows the minimum and typical buffer fanout for each TTL family. These buffers

Table XV – Fanout of CD4049A and CD4050A Buffers to TTL

	TTL Family				
Buffer Fanout	74	74H	74L	74LS	74S
Minimum	1	1	14	7	1
Typical	3	2	28	14	2

take their power from the 5-volt TTL supply and have the additional advantage of being able to accept input voltage swings of 5 to 15 volts from the preceding COS/MOS system.

In many instances, the designer may wish to use the high-speed capability of a bipolar device with the high-voltage capability of a COS/MOS device. This combination can

Table XIV – Minimum Current-Sinking Capability of COS/MOS Devices

COS/MOS Type	Description	Sink Current (mA at 25°C $V_O = 0.4$ Volt, $V_{DD} = 5$ Volt) Ceramic	Plastic
CD4000A	Dual 3-Input NOR Gate Plus Inverter	0.4	0.3
CD4001A	Quad 2-Input NOR Gate	0.4	0.3
CD4002A	Dual 4-Input NOR Gate	0.4	0.3
CD4007A	Dual Complementary Pair Plus Inverter	0.6	0.3
CD4009A/49A	Inverting Hex Buffer	3.0	3.0
CD4010A/50A	Non-Inverting Hex Buffer	3.0	3.0
CD4011A	Quad 2-Input NAND Gate	0.2	0.1
CD4012A	Dual 4-Input NAND Gate	0.1	0.05
CD4041A	Quad True/Complement Buffer	0.4	0.2
CD4031A	64-Stage Static Shift Register	1.3	1.3
CD4048A	Expandable 8-Input Gate	1.6	1.6
CD4XXXB	Any B-Type Device Output	0.4	0.4

easily be achieved by the use of the CD40109B quad low-to-high voltage level shifter, as shown in Fig. 68. The interface of the HNIL circuit enable it to interface directly with the COS/MOS input with good noise immunity.

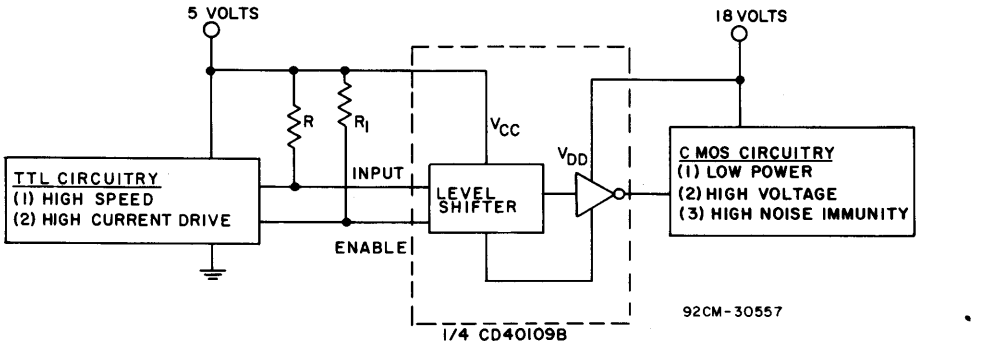


Fig. 68 — Use of level shifter for COS/MOS- to-TTL interface.

from the low-voltage circuitry (if bipolar) would have to include the resistor R to modify the inputs to the CD40109 so that they are COS/MOS-compatible.

In a system using a COS/MOS supply voltage greater than 5 volts, speed and noise immunity can be improved by use of high-voltage open-collector TTL circuits such as the 7416, 7417, or 7426, as shown in Fig. 69. The value of the pull-up resistor R_X depends on the value of V_{DD}; at 10 volts, 39 kilohms would be suitable.

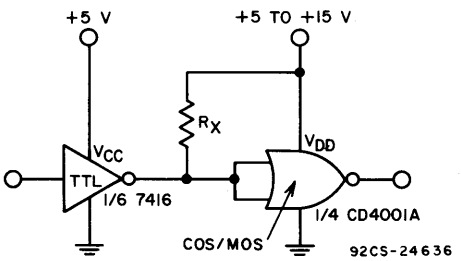


Fig. 69 — TTL-to-COS/MOS interface at a V_{DD} greater than 5 volts.

COS/MOS and HNIL

The wide operating-voltage range and low power consumption of COS/MOS circuits enable them to operate from the 12-volt power supply used for HNIL (high-noise-immunity logic) circuits. Most CD4000-series circuits will drive the HNIL input directly; in the circuit shown in Fig. 70, for example, the CD4081B output sinks the required 1.4 milliamperes at an output voltage typically less than 0.5 volt. The output-voltage levels of 0.8 volt and 10 volts

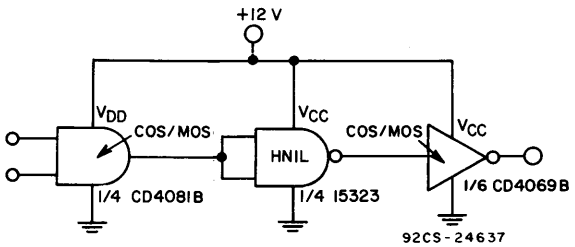


Fig. 70 — COS/MOS-to-HNIL-to-COS/MOS interface.

COS/MOS and DTL

A COS/MOS-to-DTL interface requires a buffer, such as the CD4049 shown in Fig. 71, to sink the DTL input current of 1.5 milliamperes at 0.4 volt. Fanout to DTL

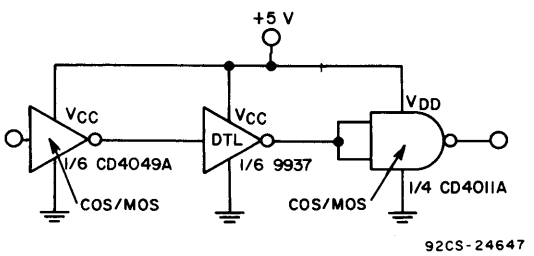


Fig. 71 — COS/MOS-to-DTL-to-COS/MOS interface.

circuits depends on the sink current capability of the COS/MOS buffer used. For the CD4049 and CD4050, typical fanout is 3.

A DTL-to-COS/MOS interface requires no special consideration because the internal pull-up resistor in DTL circuits and the extremely low input current of COS/MOS circuits assure a high logic level almost equal to the power-supply voltage.

COS/MOS and ECL

COS/MOS and ECL (emitter-coupled logic) forms can be operated from a common -5-volt (±1 V) supply. However, level-shift interface circuits are required in both directions. Fig. 72 illustrates the COS/MOS-to-ECL logic-1 and logic-0 level interface requirements.

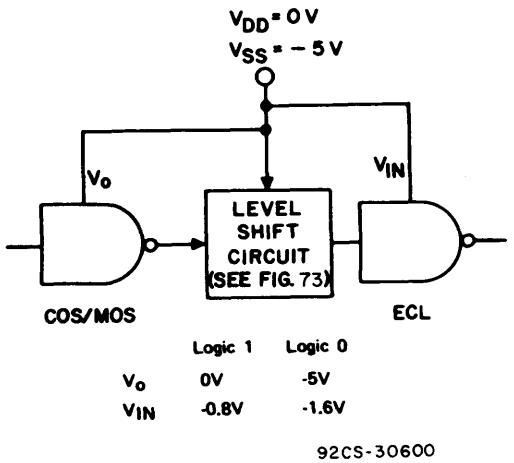


Fig. 72 – COS/MOS-to-ECL interface.

Fig. 73(a) illustrates a simple voltage-divider interface circuit. Calculation of the values of resistors R1 and R2 is based on COS/MOS source- and sink-current capability and ECL input loading. This interface suffers from poor temperature tracking and low speed. The active level translator of Fig. 73(b) has a high-speed capability and good temperature tracking.

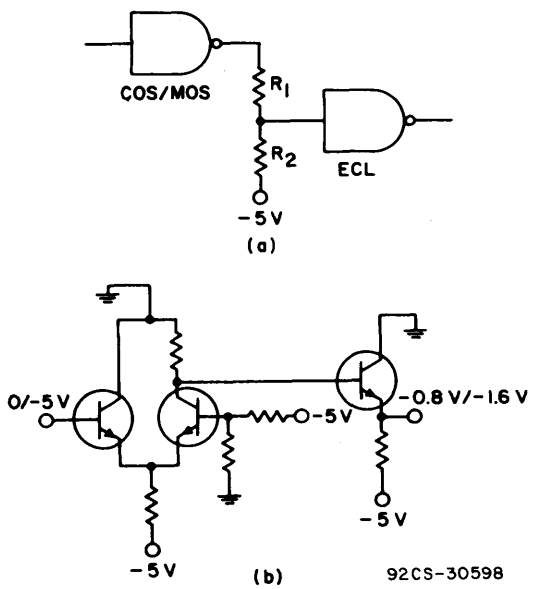


Fig. 73 – (a) COS/MOS and ECL voltage-divider interface; (b) active level translator.

An active interface circuit is required to shift from ECL output logic levels to COS/MOS logic levels. Figs. 74 and 75 illustrate logic-interface and level-shift

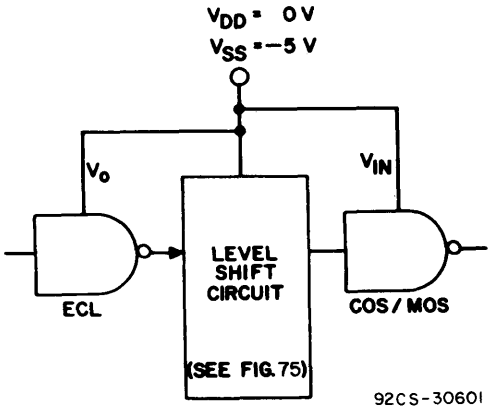


Fig. 74 – Logic interface required to shift from ECL output logic levels to COS/MOS logic levels.

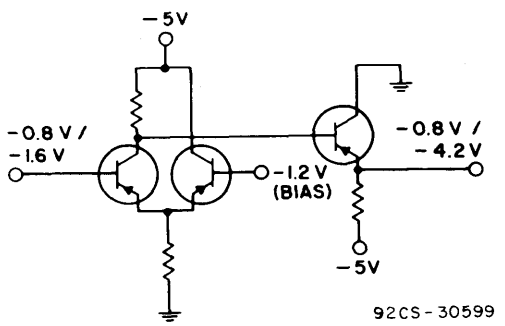


Fig. 75 – Level-shift circuit required to shift from ECL output logic levels to COS/MOS logic levels.

circuits, respectively. An important consideration in these interfaces, as well as in the COS/MOS-to-ECL interface of Figs. 72 and 73, is operation from the common -5-volt supply.

IC level shifters that translate between TTL or DTL logic levels and ECL logic levels are commercially available. Both +5-volt and -5-volt power-supply voltages must be provided when these level shifters are used. COS/MOS CD4049 and CD4050 hex

buffers may be required to drive the TTL-to-ECL level-shifter IC's. In this case, a third power supply (up to +18 volts) may be used to power the COS/MOS logic circuits.

Level Shifting

Four COS/MOS buffers (CD4009, CD4010, CD4049, and CD4050) are designed as level shifters as well as high-sink-current drivers. This important feature permits operation of COS/MOS logic at supply-voltage values up to +18 volts and direct interface with TTL or DTL circuits at +5 volts. Fig. 76 shows the schematic diagrams of the CD4009 and CD4010 buffers; V_{DD} is the COS/MOS logic-level voltage and V_{CC} is the +5-volt TTL or DTL connection. Fig. 77 shows the

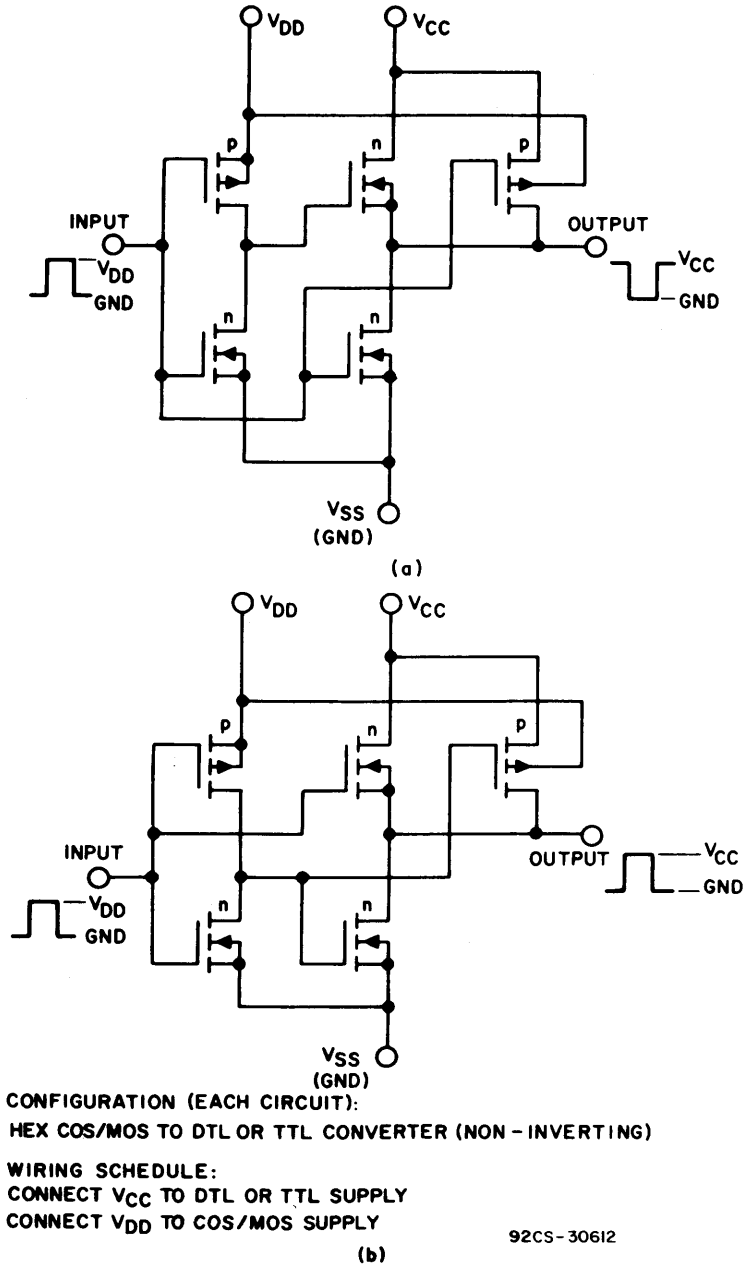


Fig. 76 – Schematic diagrams of the (a) CD4009, and (b) CD4010.

logic-interface connections for logic-level conversion. The system advantage of this configuration is manifested in the increased logic speed of COS/MOS circuits when

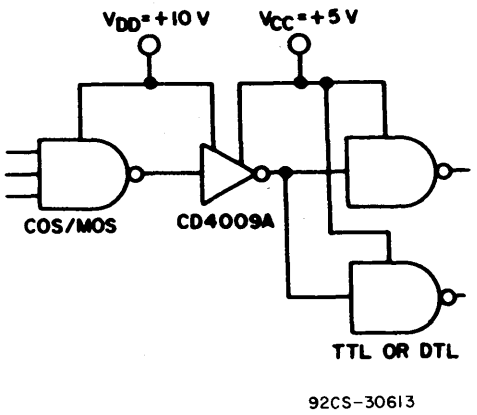


Fig. 77 — Logic-interface connections for logic-level conversion.

operated at higher speed than would be possible in an all +5-volt system. Because of their superior input protection networks, the CD4009 and CD4010 may be preferred over the CD4049 and CD4050 in extremely harsh electrical environments.

INTERFACING DISCRETE AND ELECTROMECHANICAL DEVICES

Industrial control systems employ greater logic swings than IC logic systems, such as COS/MOS, to achieve high noise immunity, to enable them to operate from readily available high-voltage supplies, and to interface with electromechanical equipment.

Fig. 78 shows a simple resistive-divider circuit used to interface a system having a 24-volt logic swing to COS/MOS. The circuit could readily be modified for even higher voltage swings. The capacitor filter enhances the excellent noise immunity of the COS/MOS logic, and the two clamp diodes keep the input signal voltage between V_{DD} and V_{SS}. An alternate circuit using a zener diode is shown in Fig. 79.

A single-transistor level converter interfacing a COS/MOS device to an industrial control system is shown in Fig. 80. The transistor is driven directly from the COS/MOS device output.

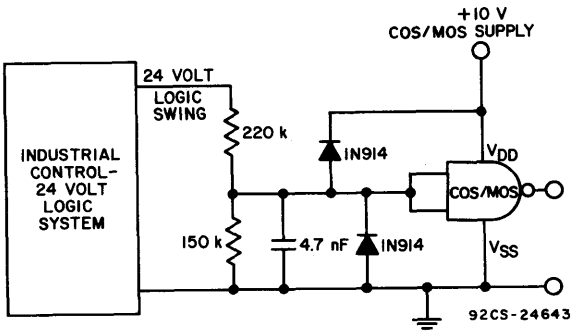


Fig. 78 — Interface from industrial control to COS/MOS.

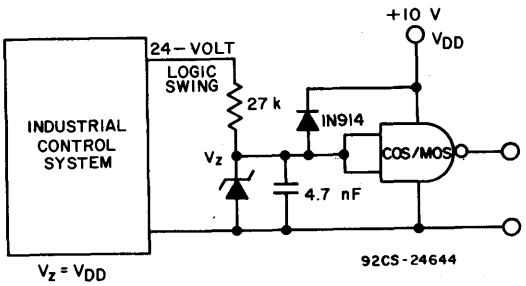


Fig. 79 — Zener-diode industrial control interface.

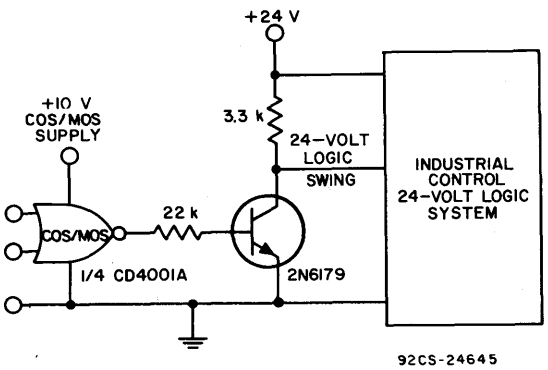


Fig. 80 — COS/MOS-to-industrial-control interface.

Schmitt Trigger Usage

The RCA-CD4093B Schmitt trigger is described in detail in Chapter VI **Astable and Monostable Multivibrators**. Two of its properties, high noise immunity and speed-up of slow pulse edges, are very useful in interfacing with industrial control circuits.

The COS/MOS CD4093B consists of four Schmitt triggers; each of the devices is a two-input NAND gate with Schmitt action on each input. The hysteresis voltage V_H shown

in Fig. 81 is typically 0.6 volt for a V_{DD} of 5 volts and 2 volts for a V_{DD} of 10 volts.

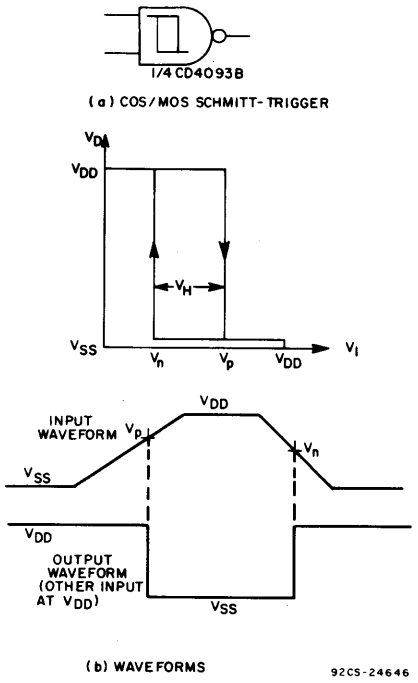


Fig. 81 — (a) COS/MOS Schmitt trigger; (b) typical waveforms for Schmitt trigger.

The noise immunity of the COS/MOS NAND Schmitt trigger is very high, typically greater than 50 percent of V_{DD} in each state. It is therefore specially suited for circuits that require a very high noise immunity. Because of the hysteresis built into the Schmitt trigger, it can tolerate noise on a slow input edge without false switching at the output, as shown in Fig. 82. This noise immunity permits the construction of an excellent

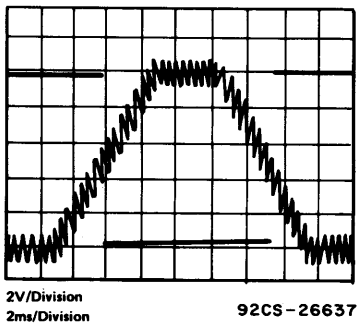


Fig. 82 — Rejection of noise on slow input edge.

interface from an industrial environment to a COS/MOS logic system, as shown in Fig. 83.

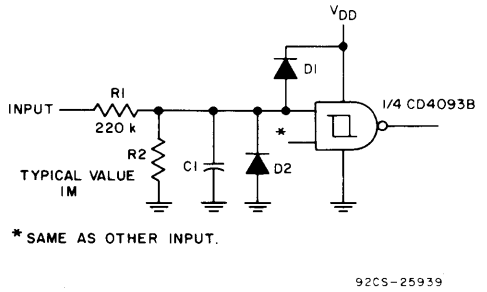


Fig. 83 — Industrial-environment-to-COS/MOS interface.

The CD4093B will function under the most severe conditions of input overvoltage and in spite of noise spikes up to hundreds of volts. The input is kept between V_{SS} and V_D by clamp diodes D1 and D2; R1, typically 220 kilohms, functions as a current-limiting resistor. Resistor R2 ties the logic input to V_{SS} in the event that the interface input is accidentally open-circuited, for example by the removal of a PC board from a system. Capacitor C1, in conjunction with R1, acts as a filter and enhances the noise-rejection properties of the interface.

Solenoid Drives

A high-power coil such as the solenoid of a printer hammer, which requires about 1 ampere at 70 volts, may be driven from a COS/MOS system by use of a Darlington transistor, as shown in Fig. 84. Because a typical value of V_{BE} for a type 2N6385 transistor is 1.5 volts at a collector current of 1 ampere and a minimum gain of 1000, the output source transistor of the CD4073B has to supply 1.5 milliamperes. The value of resistor R is selected so that V_{DS} is sufficient to assure this output current. Suitable values of R for use with B-series types are given in Fig. 84 for V_{DD} values of 5, 10, and 15 volts.

SCR and Triac Drives

MOS outputs. A sensitive-gate SCR such as the 106B1 controlling directly 2.5 amperes at reverse voltages up to 600 volts may be controlled directly by a COS/MOS gate such as the CD4069B, as shown in Fig. 85.

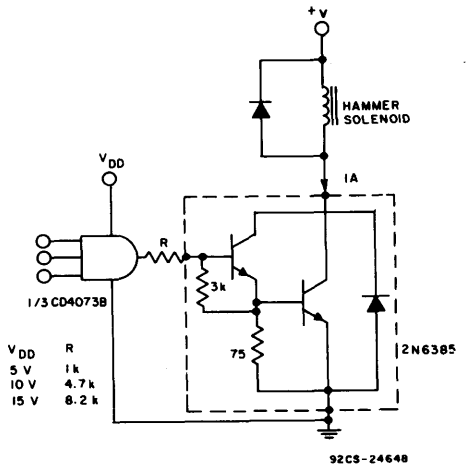


Fig. 84 – COS/MOS system driving a printer-hammer solenoid with the aid of a Darlington transistor.

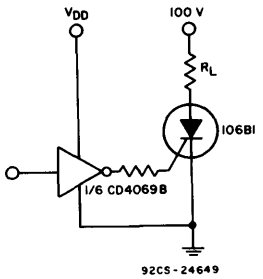


Fig. 85 – COS/MOS gate directly driving a sensitive-gate SCR.

SCR's and triacs with gate currents in the milliampere region may be controlled by a buffer such as the CD4049. This buffer could, in turn, be controlled by a COS/MOS system or, as shown in Fig. 86, by an opto-coupler to provide greater isolation.

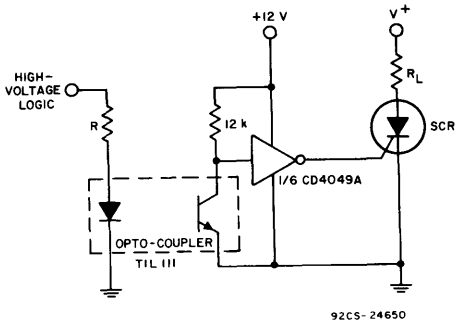


Fig. 86 – High-voltage logic to COS/MOS driving an SCR.

In cases where a single-gate output source or sink current is sufficient, the inputs and outputs of gates on the same chip can be paralleled, as shown in Fig. 87. Gates not on

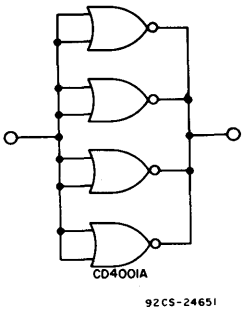


Fig. 87 – Paralleling inputs and outputs.

the same chip and buffer circuits should not be operated in parallel because variations in transition-point voltage may cause over-dissipation.

Relay Drives

The CD4049 buffer may be used to drive a sensitive relay directly, as shown in Fig. 88. Typically, the relay would have a coil resistance of 1100 ohms, and a nominal coil current of 10.9 milliamperes. Operating at 12 volts, the n-channel transistor in the CD4049 would sink the current with a voltage drop of only 0.7 volt. An external diode D1 connected between the output and $+V_{DD}$ protects against high transient switching voltages. A similar high-current drive device, CD40107, is available for high-sink-current applications.

INTERFACING OP-AMPS TO COS/MOS

COS/MOS circuits may be connected directly to the output of an operational amplifier operating between the normal 15-volt supply rails, as shown in Fig. 89, provided clamp diodes to V_{DD} and V_{SS} are used to make sure the COS/MOS input voltage does not go outside the V_{SS} and V_{DD} range. Resistor R3 limits the op-amp

output current in the event that the op-amp output voltage tends toward the negative rail. Fig. 90 shows a CA741-type op-amp operated between V_{DD} and V_{SS} with a resistive divider on the non-inverting op-amp input.

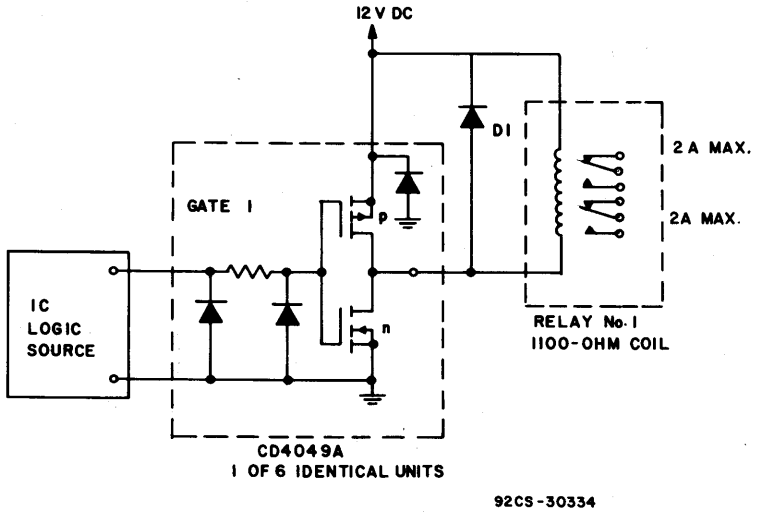


Fig. 88 – COS/MOS buffer driving a sensitive relay.

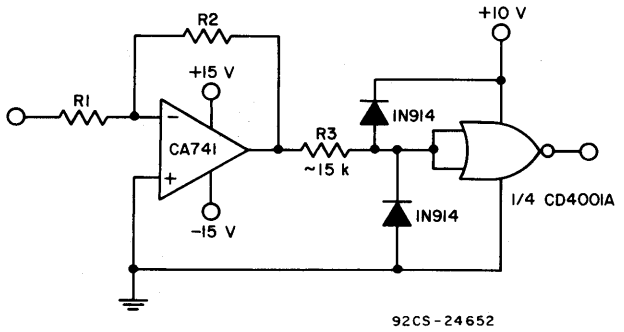


Fig. 89 – Interface from split-rail op-amp to COS/MOS gate.

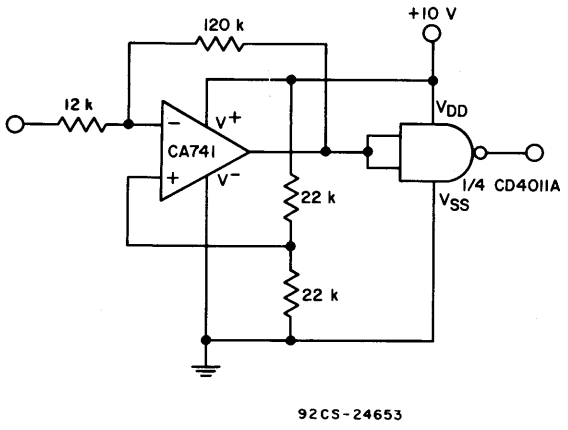


Fig. 90 – Interface of op-amp and COS/MOS with common supply rail.

VI. Astable and Monostable Multivibrators

COS/MOS devices provide the advantages of cost and size reductions in multivibrator circuits because their high input impedance makes it possible to obtain large time constants without the use of large capacitors.

ASTABLE CIRCUITS

The simplest astable multivibrator circuit consists of two inverters, one resistor, and one capacitor, as shown in Fig. 91. The inverter configuration can be obtained from either NAND or NOR gates by tying all the inputs together. When the waveform at the output of inverter B (waveform 1 in Fig. 91(b)) is in a high or "one" state, the capacitor C_{tc} charges positive. As a result, the input to inverter A (waveform 2) is high and the output of A (waveform 3) is low or "zero". The resistor R_{tc} is returned to the output of inverter A to provide a path to ground for discharge of the capacitor.

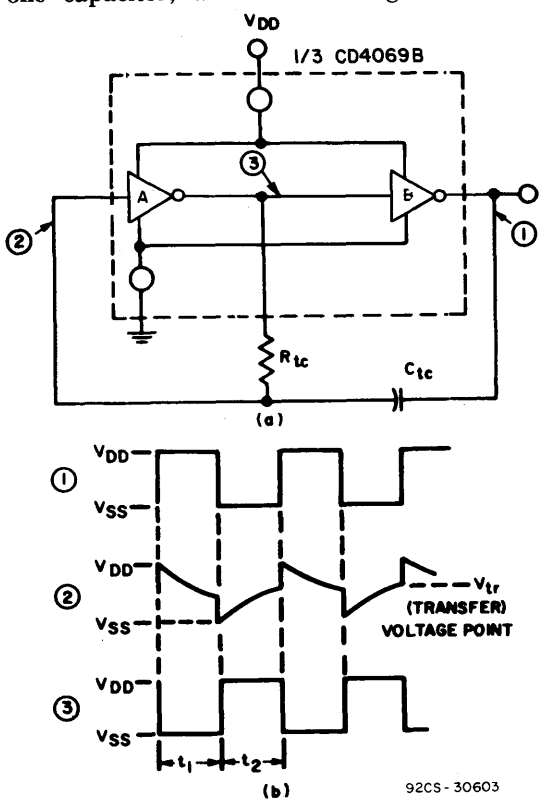


Fig. 91 – Astable multivibrator circuit using two COS/MOS inverters: (a) circuit diagram, and (b) voltage waveforms.

As long as the output of inverter A is low, the output of inverter B is high. As capacitor C_{tc} charges, however, the voltage generated (waveform 2) approaches and passes through the transfer-voltage point of inverter A. At the instant that this crossover occurs, capacitor C_{tc} starts to discharge causing the output of A (waveform 3) to become high. As a result, the output of B (waveform 1) becomes low. The resistor R_{tc}, connected to the output of A, then provides a discharge path to the supply voltage. As capacitor C_{tc} discharges, voltage waveform 3 again approaches and passes through the transfer-voltage point of inverter A. At that instant, the circuit again changes state (the output of A becomes low and that of B high), and the cycle repeats.

Improved Circuit

Adding a resistor in series with the input lead to inverter A, as shown in Fig. 92, reduces the variation in the time period with transfer voltage (this variation can be as much as 33 percent from unit to unit). The resistor also makes the frequency independent of supply voltage. The value of the series resistor R_s

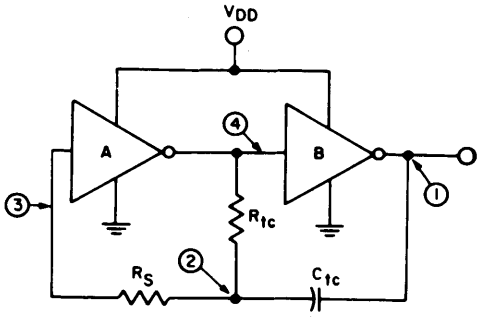


Fig. 92 – COS/MOS inverter with resistor in series with one input to make circuit independent of supply-voltage variations.

should be at least ten times that of the resistor R_{tc} to allow the waveform generated at the resistor-capacitor junction to rise to $V_{DD} + V_{tr}$ (the transfer voltage).

The multivibrator can be gated on and off under control of a logic signal if a NAND or NOR gate is used for the first inverter. A gated multivibrator circuit is shown in Fig. 93.

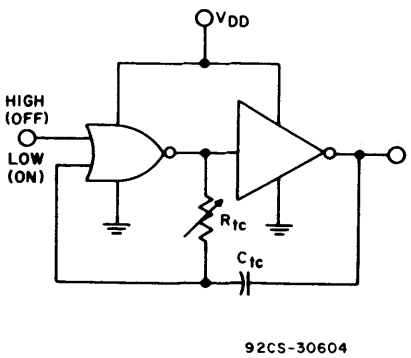


Fig. 93 – Astable multivibrator in which a NOR gate is used as the first inverter to permit gating.

The CD4047 as an Astable Multivibrator

Although the multivibrator circuits described above can easily be constructed using the CD4007 dual complementary pair plus inverter, the CD4093 Schmitt trigger, the CD4001 quad 2-input NOR gate, the CD4011 quad 2-input NAND gate, or many other COS/MOS devices, improved performance can be achieved by using the integrated oscillator section of the CD4047 multivibrator, as shown in Fig. 94. This circuit requires only a single resistor and a single capacitor for operation. It has the same time period and stability as the circuit shown in Fig. 92 when the value of R_s is infinite.

The primary reason for the improved performance of the CD4047 circuit is the special input-protection of the device, which allows the capacitor-charging waveform to swing above V_{DD} and below V_{SS}. As a result, the waveform is not clipped and more accurate timing occurs. In addition, variations in characteristics are reduced.

The CD4047 also provides the following other performance advantages:

1. The transfer voltage point of the input inverter A in Fig. 94 is tested between 33 and 67 percent of V_{DD} instead of between 30 and 79 percent; this narrower test range improves stability by reducing unit-to-unit variation.

2. Large buffers are used for inverters D and E to reduce the effect of changes in device output impedance with period stability.

3. Power dissipation is reduced, compared to that of the multivibrator circuits

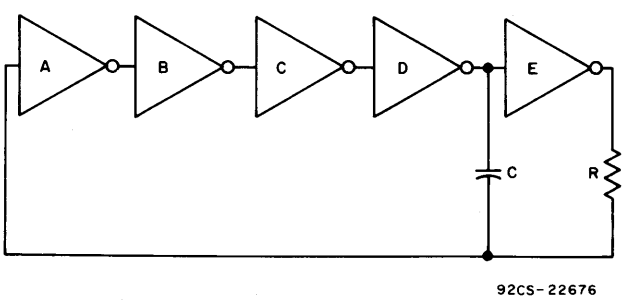


Fig. 94 – CD4047 oscillator section.

using gate and inverter devices previously discussed. This reduction is achieved because inverter A of the integrated circuit is designed with high-impedance components so that during the time that the inverter operates in the middle of its transfer region (both p-channel and n-channel devices on), current flow from V_{DD} to V_{SS} is limited. The inverters which follow A gradually shift from high-impedance types to the very-low-output-impedance driver.

MONOSTABLE CIRCUITS

Fig. 95(a) shows a basic "one-shot" circuit that uses a single RC time constant. This circuit operates well provided R_{tc} and C_{tc} are adjusted to the particular COS/MOS unit used. If no adjustment is made, the period T can vary from unit to unit by as much as -40 percent to +60 percent if the transfer voltage varies by ± 33 per cent, as shown by the waveforms in Fig. 95(b).

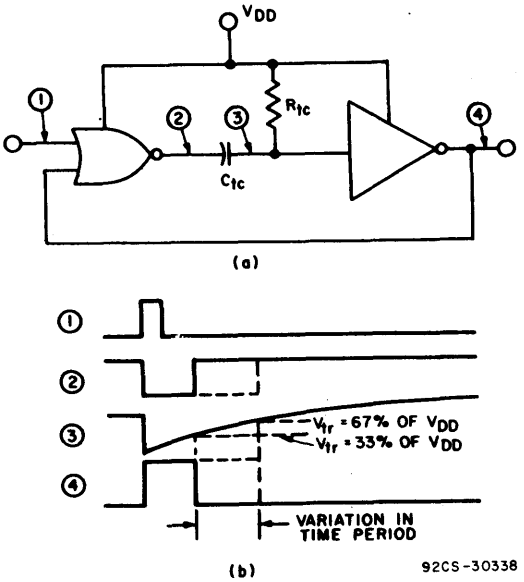


Fig. 95 — Basic one-shot multivibrator circuit: (a) circuit diagram, and (b) waveforms.

Compensated Circuit

Fig. 96 shows a compensated multivibrator circuit that can be triggered with a negative-going pulse (V_{DD} to ground). The advantage of using two inverters fabricated on the same chip in this type of circuit is that they have similar transfer voltages. When two equal RC time constants are used (R1C1 = R2C2), the effects of variations in transfer voltage from device to device are effectively cancelled out, as shown in Fig. 97. The maximum variation in transfer voltage in the time period T is less than 9 per cent. The total time for one period T1 is approximately 1.4 times the R1C1 time constant. Unlike the astable multivibrator circuit, which shows no variation in frequency with temperature, the monostable multivibrator shows a change in time period up to 10 per cent over the temperature range from -55°C to +125°C.

Figs. 98 and 99 show two variations of the monostable circuit, together with their associated waveforms. The circuit of Fig. 98 triggers on the negative-going excursions of the input pulse. The output pulse is positive-going and is taken from the first inverter. This circuit needs no external diode. The circuit of Fig. 99 triggers on the positive-going excursion of the input pulse, and then locks back on itself until the RC time con-

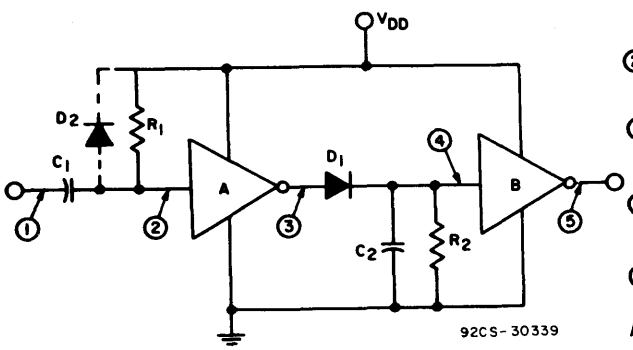


Fig. 96 — Compensated monostable multivibrator circuit.

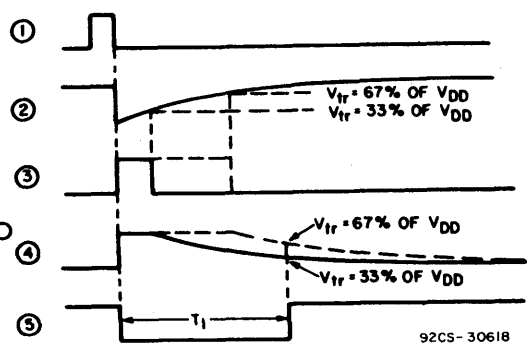


Fig. 97 — Waveforms showing the cancelling effects of transfer-voltage variations of the two COS/MOS inverters when two equal time constants are used.

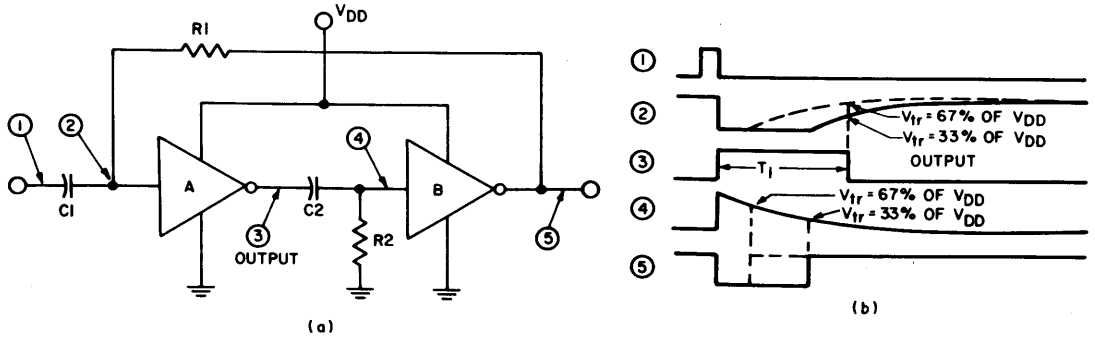


Fig. 98 — Monostable multivibrator that is triggered by a negative-going input pulse: (a) circuit diagram, and (b) waveforms.

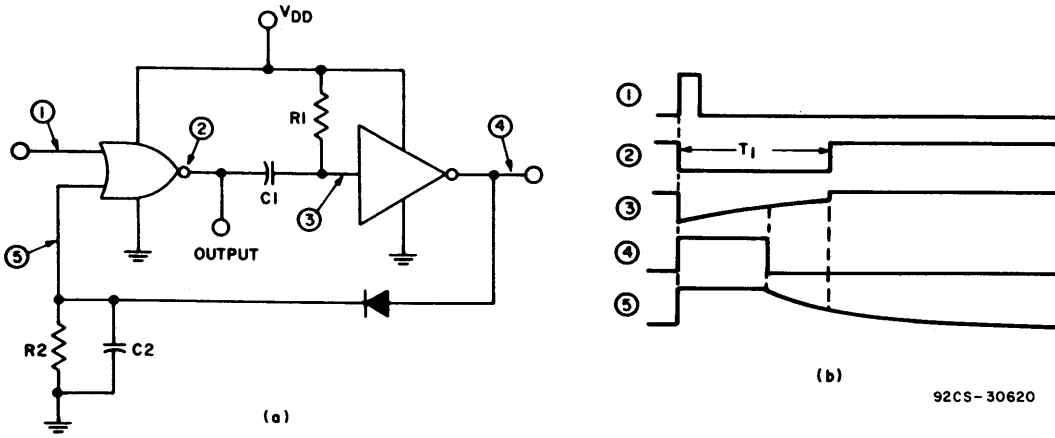


Fig. 99 — Monostable multivibrator that is triggered by a positive-going input pulse: (a) circuit diagram, and (b) waveforms.

stants complete their discharge. The circuits of Figs. 98 and 99 cannot be retriggered until they return to their quiescent states.

Low-Power Circuits

The monostable circuits discussed thus far dissipate some power because one or both of the inverters are on during the charging or discharging of the RC time constants. This power dissipation can be minimized by keeping the "one-shot" pulse width short compared to the over-all cycle time.

COS/MOS INTEGRATED ONE-SHOTS

The RCA-CD4047 is a low-power integrated COS/MOS monostable/astable multivibrator circuit. The oscillator section of the CD4047 was described previously. Fig. 100 shows the complete logic block diagram.

When the CD4047 is used in the monostable mode, it provides several advantages over discrete designs. A high degree of accuracy can be achieved with one time constant, and power dissipation is lower than with discrete designs. The logic diagram of Fig. 101 shows that many functions can be achieved with the CD4047, including leading- and trailing-edge triggering, and retriggering.

A clamping circuit is provided on the CD4047 chip, as shown in Fig. 102, to reduce the recovery time (t_r) that would normally exist in other monostable circuits. Fig. 103 shows the effect of this clamping circuit on the one-shot RC waveform. Fig. 104 shows the monostable-pulse-width stability as a function of duty cycle for specific R and C external components. There is no appreciable change in pulse width until the duty cycle approaches 100 per cent.

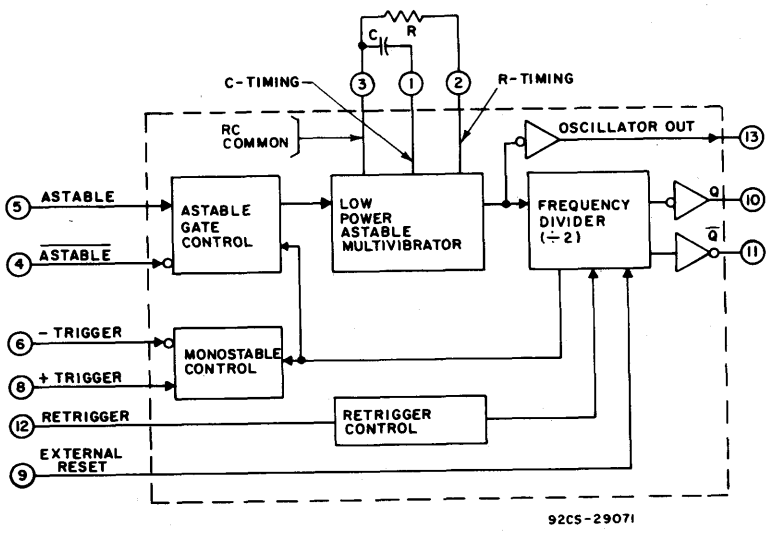


Fig. 100 – CD4047 logic block diagram.

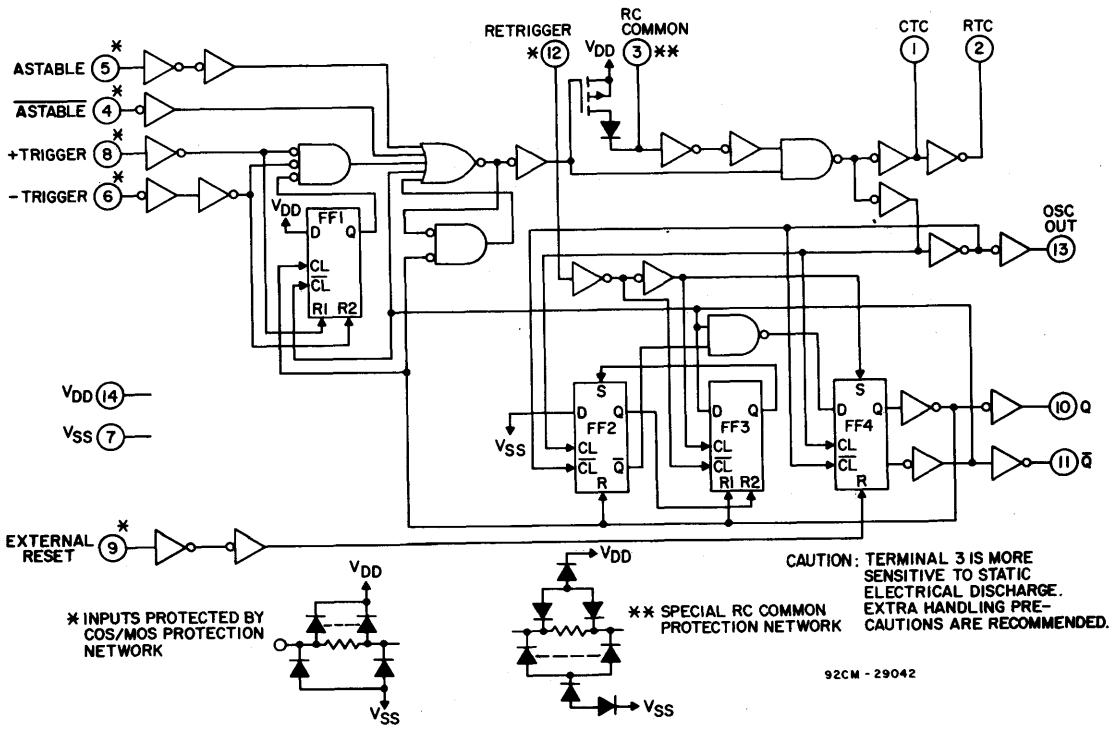


Fig. 101 – CD4047 logic diagram.

A disadvantage of the clamping circuit is that it introduces additional capacitance at the RC common node (pin 3), which may be noticeable for short pulse widths in the monostable mode only. Some diffusion capacitance present at the base of the n-p-n transistor is used to charge the capacitor C to V_{DD} quickly after the one-shot cycle has terminated. This capacitance is multiplied by the beta of the transistor and is in parallel

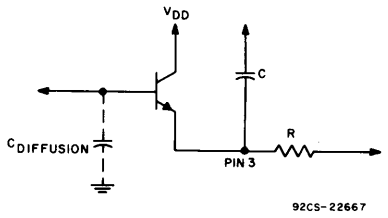


Fig. 102 – CD4047 clamping circuit.

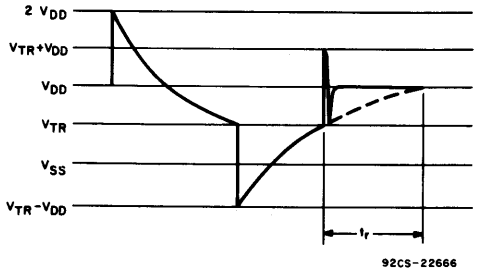


Fig. 103 – CD4047 one-shot RC waveform.

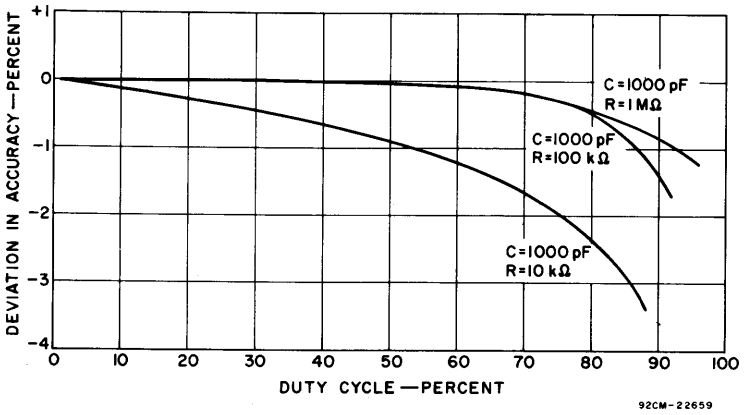


Fig. 104 – CD4047 monostable accuracy as a function of duty cycle.

with the external capacitor C during the time interval that the transistor is on ($V_{DD} - V_{BE} < t < V_{BE}$). As a result, when values of C less than 1000 picofarads are used, the actual pulse width is longer than may have been calculated. Fig. 105 shows actual typical pulse widths as a function of external capacitance. The minimum values of C shown in the graph are the smallest that can be used with the CD4047 to assure proper operation of the circuit.

SCHMITT-TRIGGER MULTIVIBRATOR CIRCUITS

The COS/MOS Schmitt trigger circuit CD4093B accepts inputs with slow rise and fall times and produces output waveforms with very fast edges. It has higher ac and dc noise immunity than other COS/MOS gates and a lower power dissipation for comparable slow-input signals. Because of these features, it can be used to advantage in multivibrator circuits.

CD4093B Characteristics

The RCA-CD4093B consists of four Schmitt triggers, as illustrated in the functional diagram of Fig. 106. Each of the four devices is a two-input NAND gate with Schmitt action on each input, yielding a typical hysteresis voltage of 2 volts with a 10-volt supply without the need for any external components.

Fig. 107 shows the logic diagram for one of the four Schmitt triggers in the CD4093B. Each input has the standard COS/MOS input protection network and each output is double buffered.

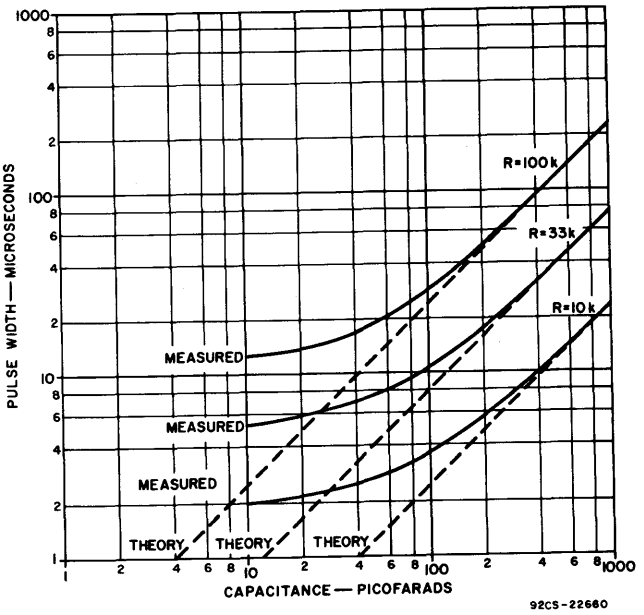


Fig. 105 – CD4047 pulse width as a function of capacitance.

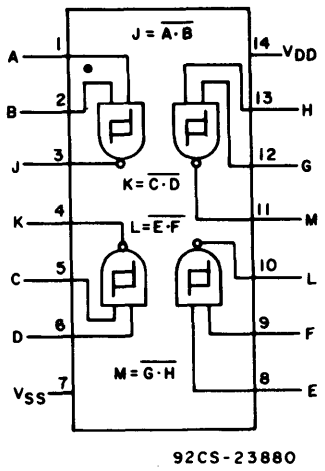


Fig. 106 – CD4093B Schmitt trigger functional diagram.

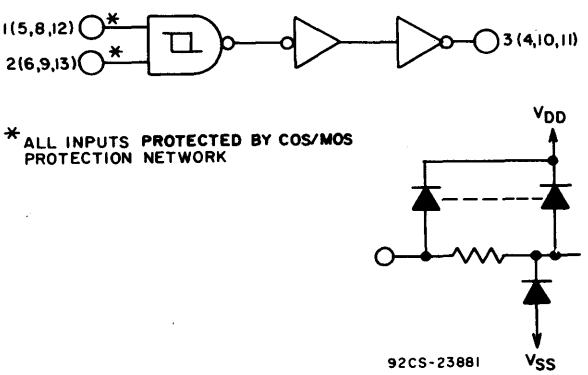


Fig. 107 – Logic diagram for one of the four Schmitt triggers in the CD4093B.

Fig. 108 shows the transfer characteristic of the Schmitt trigger. The general shape of this characteristic is the same for all values of V_{DD}, but the relative values of the positive-going signal switching point V_P, the negative-going signal switching point V_N, and the difference between them V_H (or the hysteresis voltage) change with V_{DD}. As the input is increased from zero (V_{SS}), the output remains high (V_{DD}) until V_P is reached. At this point the output goes low

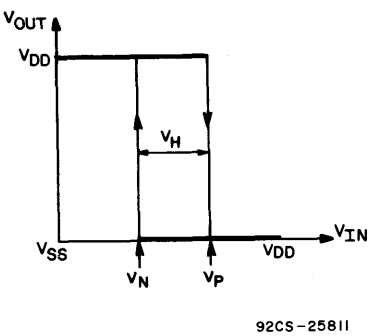


Fig. 108 – Transfer characteristic of the CD4093B Schmitt trigger.

(V_{SS}) and remains low as the input voltage is raised to V_{DD}. If the input voltage is then reduced, the output stays low (V_{SS}) until V_N is reached. At this point the output goes high (V_{DD}) and remains high as the input voltage is reduced to zero (V_{SS}). The hysteresis voltage V_H is typically 0.6 volt for a V_{DD} of 5 volts and 2 volts for a V_{DD} of 10 volts. Fig. 109 shows typical hysteresis voltage as a function of supply voltage.

noise immunity in each state exceeds the supply voltage for pulses shorter than 200 nanoseconds. The energy noise immunity is the product of noise-pulse voltage, noise-pulse time, and the appropriate value of the output drive current for the device under test; the units of energy are nanojoules (10^{-9} joule). At each value of supply voltage, the curves in Fig. 112 show a minimum value. The value of the minimum energy noise

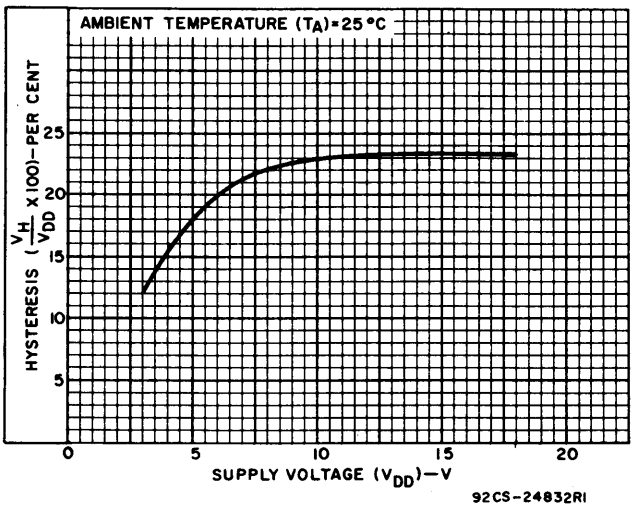


Fig. 109 – Typical hysteresis as a function of supply voltage.

Fig. 110 shows the input/output characteristics of the CD4093B; the output characteristic shown is the same for any COS/MOS device, including the Schmitt trigger. The input characteristic is unique to the Schmitt trigger and shows that when the CD4093B is driven by another COS/MOS device it has more than 50-per-cent noise immunity in each state.

Figs. 111 and 112 show measurements of voltage and energy noise immunity for the Schmitt trigger. For a V_{DD} of 5 volts, the immunity increases with increasing V_{DD} and occurs at a lower value of noise-pulse width.

Another important property of the Schmitt trigger is illustrated in Fig. 113, which compares the supply current consumed by the CD4093 with that used by the CD4011 when the input has long rise and fall times. The power dissipated by the Schmitt trigger is clearly much less than that dissipated by the quad NAND gate. Consequently, the Schmitt trigger should be used in ap-

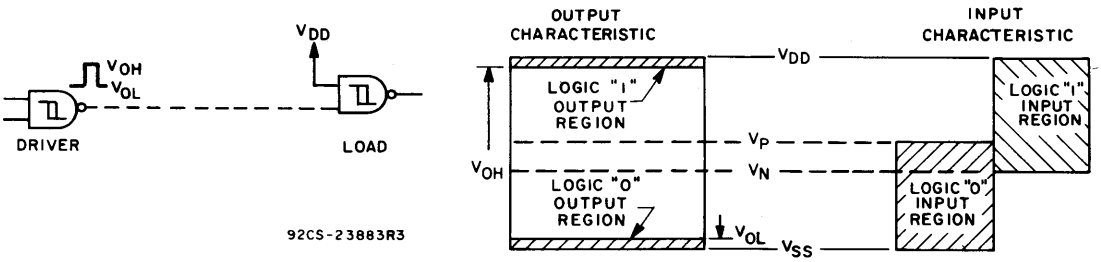


Fig. 110 – Input and output characteristics of the CD4093B.

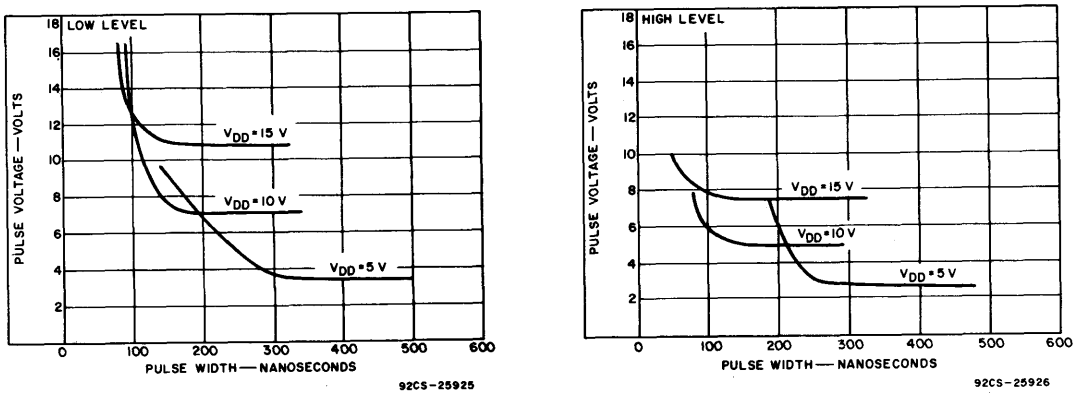


Fig. 111 – Voltage noise immunity of the CD4093B.

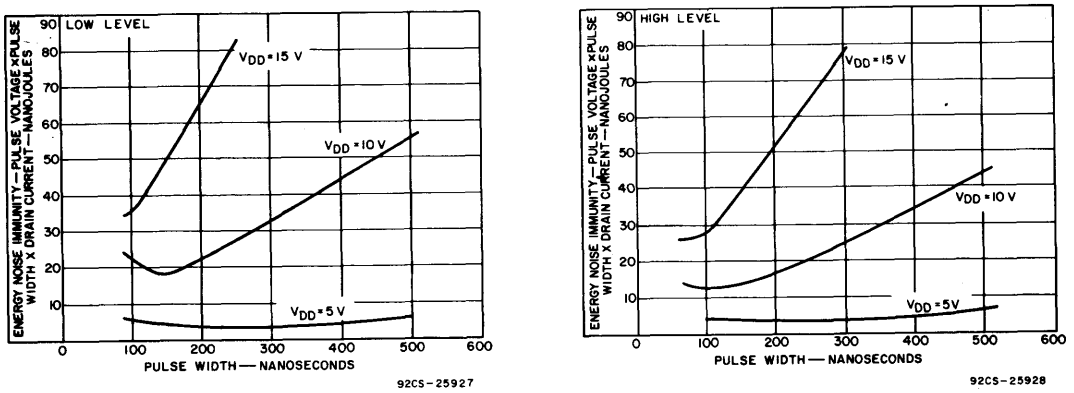


Fig. 112 – Energy noise immunity of the CD4093B.

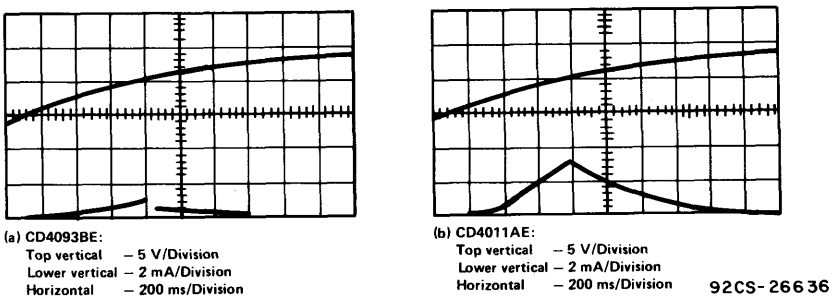


Fig. 113 – Power consumption with slow input edge for the CD4093 and the CD4011.

plications in which slow input edges are anticipated.

Slow edges are a common phenomenon in digital systems. Examples include the output from a transducer, the output at the end of a long line, an output with large capacitive load, or the output of a filter. The Schmitt trigger is particularly useful in these applications in generating a waveform with fast edges. Fig. 114 illustrates the sharpening-up capability of the Schmitt trigger. With an input edge time of 8 milliseconds and an output transition time of 100 nanoseconds, the improvement in edge time is a factor of 10^7. With longer input edge times the improvement is even greater.

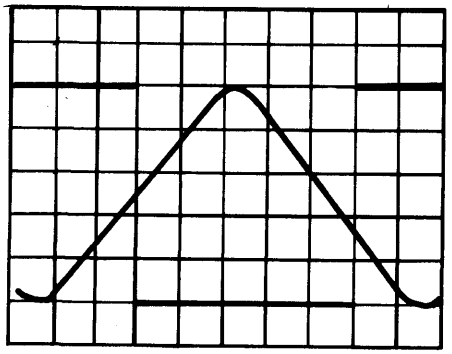


Fig. 114 – Sharpening up a slow edge.

Schmitt-Triggered Astable Oscillators

A range of astable oscillators may be easily constructed using the CD4093B COS/MOS quad 2-input NAND Schmitt trigger. Fig. 115 shows the basic circuit and the waveforms associated with it. In this circuit, input and output are at ground potential and capacitor C is discharged before power is applied. When power is applied, the output goes high (V_{DD}) and capacitor C charges through resistor R until V_P is reached; the output then goes low (V_{SS}). C then discharges through R until V_N is reached. At this point the output goes high and C again charges through R until it reaches V_P. Thus, the voltage at point A alternately swings between V_P and V_N as the output (B) goes high and low.

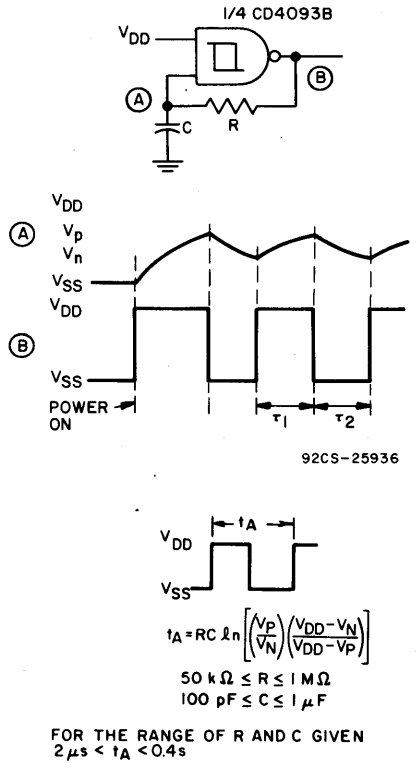


Fig. 115 – CD4093B astable multivibrator.

Schmitt-Triggered Monostable Multivibrators

A typical circuit for a monostable multivibrator using the CD4093B Schmitt trigger is shown in Fig. 116. Monostable operations starts with both inputs high and the output low. A positive pulse turns on the n-channel device in parallel with capacitor C, causing C to discharge through the now low shunt impedance. When the voltage at input point 2 drops to V_N the output goes high. When the input pulse goes low, the n-channel device turns off, opening the shunt impedance. Capacitor C then starts to charge through resistor R; when the voltage at input point 2 reaches V_P the output goes low.

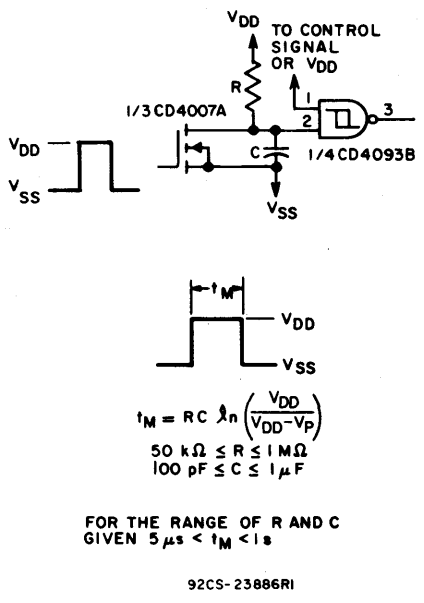


Fig. 116 – CD4093B monostable multivibrator.

VII. Crystal Oscillators for Digital Timekeeping

This chapter on crystal oscillators, together with the two following chapters (VIII. Shift Registers and Counters, and IX. Display Drivers), covers the basic elements of digital timekeeping and the use of COS/MOS devices in electronic watches and clocks.

Quartz crystal oscillators have excellent frequency stability and can be used over a wide range of frequencies. COS/MOS crystal-oscillator circuits provide the additional advantages of low power consumption and stable operation over a wide range of supply voltages. Such oscillators are well suited to digital timekeeping applications.

BASIC OSCILLATOR DESIGN CONSIDERATIONS

A basic oscillator circuit consists of an amplifier and a feedback section, as shown in Fig. 117. For oscillation to occur, the gain (α) of the amplifier times the attenuation (β) of the feedback network must be greater than unity (i.e., $\alpha\beta > 1$). In addition, the total phase shift through the amplifier and feedback network must be equal to n times 360 degrees, where n is an integer. These conditions imply that oscillations occur in any system in which an amplified signal is returned in phase to the amplifier input after being attenuated less than it was originally amplified. In such a system, any noise present at the amplifier input causes oscillation to build up at a rate determined by the loop gain (or $\alpha\beta$ product) of the over-all circuit.

The frequency stability of an oscillator depends primarily on the phase-changing (or frequency-selective) properties of the feedback network. For high stability, quartz crystals and tuning forks are commonly used as feedback network elements. The quartz crystal is the more popular because of its higher Q or greater inherent frequency stability.

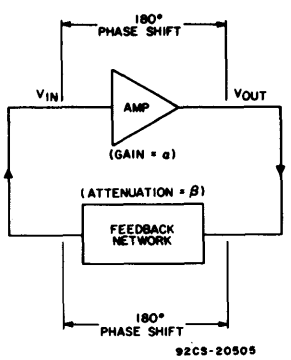


Fig. 117 – Basic oscillator circuit.

Selection of Crystal Operating Mode

Fig. 118 shows the equivalent circuit of a quartz crystal, and Table XVI lists typical

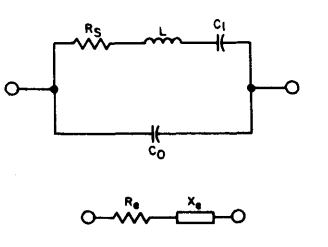


Fig. 118 – Equivalent circuit for a quartz crystal.

Table XVI – Typical Component Values for Common Cuts of Quartz Oscillator Crystals

FREQUENCY	32 kHz	280 kHz	525 kHz	2MHz
Cut	XY Bar	DT	DT	AT
R_S (ohms)	40K	1820	1400	82
L (Hy)	4800	25.9	12.7	0.52
C_1 (pF)	0.00491	0.0125	0.00724	0.0122
C_o (pF)	2.85	5.62	3.44	4.27
C_o/C_1	580	450	475	350
Q	25000	25000	30000	80000

component values of the elements included in the equivalent circuit for different crystal cuts and operating frequencies. The basic circuit can be resolved into equivalent resistive (R_e) and reactive (X_e) components. Fig. 119 shows curves of these components as functions of frequency for a typical 32.768-kHz crystal and a crystal load capacitance C_L of 10 picofarads. Fig. 119(b) indicates that there are two points at which the crystal appears purely resistive (i.e., points at which $X_e = 0$). These points are defined as the resonant (f_r) and antiresonant (f_a) frequencies. Series-resonant oscillator circuits are designed to oscillate at or near f_r. Parallel-resonant circuits oscillate between f_r and f_a, depending on the value of a parallel loading capacitor C_L (as discussed later). In contrast to series-resonant circuits parallel-resonant circuits work best with amplifiers that have high input impedances. As a result, parallel-resonant circuits are most applicable to crystal oscillators that employ COS/MOS amplifiers.

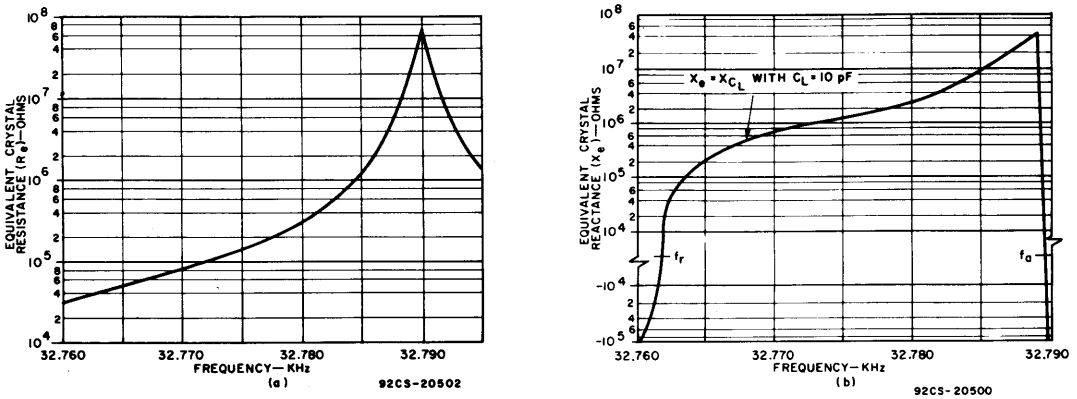


Fig. 119 – Impedance characteristics of a quartz crystal: (a) equivalent crystal resistance as a function of frequency; (b) equivalent crystal reactance as a function of frequency.

Feedback-Circuit Configuration

A feedback circuit suitable for use with a parallel-resonant oscillator circuit is shown in Fig. 120. This circuit, known as a crystal pi network, is intended for use with an amplifier that provides a 180-degree phase shift. The pi network is designed to provide the additional

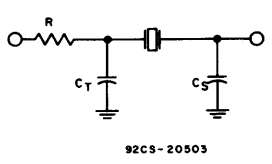


Fig. 120 – Crystal pi-type feedback network.

180-degree phase shift required for oscillation. The phase angle for this type of feedback circuit is extremely sensitive to a change in frequency, a condition necessary for stable oscillation. If the equivalent resistance of the crystal were in fact zero (infinite Q), a change in the phase angle of the feedback circuit would not cause in oscillator frequency. The frequency, therefore, would be insensitive to any change in the amplifier.

Although practical crystals allow only a slight change in frequency for large variations in phase angle, the amplifier phase angle should, to the extent possible, be made independent of temperature and supply-voltage variations in order to minimize the phase compensation required of the feedback network. Any required phase compensation will, of course, dictate a corresponding change in the frequency of oscillation consistent with practical values of crystal Q. For this reason, the equivalent resistance of the crystal should be maintained as low as possible, and the amplifier should be designed to roll off at frequencies greater than the crystal frequency.

Oscillator Amplifier

Fig. 121 shows a COS/MOS amplifier circuit that may be used to provide the amplification function in a crystal-controlled oscillator.

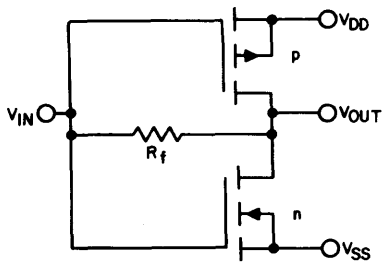


Fig. 121 – COS/MOS amplifier.

The MOS devices can be part of the CD4007 dual complementary pair plus inverter. The amplifier is biased so that the output voltage V_{OUT} is equal to the input voltage V_{IN}, or typically is equal to one-half the supply voltage V_{DD} (i.e., $V_{OUT} = V_{IN} = V_{DD}/2$). Biasing is accomplished by means of a resistor that has a value high enough to prevent loading of the feedback network, yet low in comparison to the amplifier input resistance. Resistor values of 10 to 500 megohms satisfy these criteria. Values at the lower end of this range, in the order of 15 megohms, are generally used to allow greater input leakage without any severe change in bias point.

The gain of the amplifier varies with supply voltage, the size of the n-channel and p-channel MOS transistors, and the sum of the threshold voltages of the transistors. When an oscillator amplifier is designed to roll off at frequencies greater than the crystal frequency, care must be taken to make sure that the transistors are large enough for the particular supply voltage used and the range of threshold voltages expected. For any circuit, however, the sum of the threshold voltages of the n- and p-channel transistors must always be less than the supply voltage.

To a certain extent, the oscillator amplifier governs the selection of the components for the feedback network. The amplifier current consumption depends strongly on the attenuation across the feedback network. As the attenuation becomes greater, the signal at the amplifier input becomes smaller, and the amplifier current increases considerably. Large voltage swings at the amplifier input cause negligible current because the resistance of either the n-channel or the p-channel transistor is high during a large portion of the cycle. On the basis of power considerations, it is best to design the feedback network for a small attenuation.

Equivalent Crystal Resistance

The equivalent resistance R_s of the crystal should be as small as possible in order to obtain minimum attenuation across the feedback network. For any given circuit, the oscillator current always increases with a rise in crystal resistance. This factor and stability considerations provide strong arguments for the use of crystals that have low series resistance, although the usual cost tradeoffs prevail.

Crystal Load Capacitance

Another factor that influences the over-all power consumption is the value of the pi-network capacitor C_T at the amplifier output. For minimum current consumption,

this capacitor obviously should be kept small. However, low capacitance does not always imply high frequency stability. The choice of the capacitor value first involves a determination of the over-all crystal load capacitance. The phase angle of the feedback network approaches 180 degrees when the crystal equivalent reactive component X_e is equal to the reactance (X_{CL}) of a capacitor placed in parallel with the crystal. Fig. 120 shows that the effective capacitance across the crystal consists of the two pi-network capacitors in series. If the value of the equivalent reactance X_e at the crystal frequency, as determined from Fig. 119(b), is equal to the value of the crystal load capacitance C_L, then the equivalent value of the two series-connected pi-network capacitors can be calculated from the following relationship:

$$C_L = 1/\omega X_e$$

The value of the load capacitance C_L is generally selected first, and the crystal manufacturer is required to cut the crystal to oscillate at the desired frequency for the specified value of load capacitance.

The choice of a load capacitance is important in terms of over-all power consumption and frequency stability. Higher values of C_L generally improve frequency stability, but also increase power dissipation. The timing industry presently seems to have standardized on values of C_L between 10 and 20 picofarads.

The choice of the total equivalent load capacitance C_L only fixes the series sum of the two pi-network capacitors C_T and C_S. The values of the individual capacitors can be determined from the following expressions:

$$C_T = 4\,C_L/(1 - 5fR_eC_L)$$

$$C_S = 4\,C_L/(3 + 5fR_eC_L)$$

The actual value of C_S used in the feedback circuit should be about 7 picofarads less than the calculated value to allow for the amplifier input capacitance. The value of the amplifier output capacitor C_T should not normally be fixed. A trimmer capacitor should be placed in parallel with, or used in place of, a fixed output capacitor to compensate for variations in stray capacitance and circuit components. The mid-range value of the output capacitor (or combination) should be equal to the calculated value of C_T.

Frequency-Trimming Capability

The required capacitance range for the oscillator trimmer capacitor is determined by the variation in oscillation frequency with a change in load capacitance. The total frequency-trimming range of a crystal-controlled oscillator circuit is primarily a function of the crystal characteristics or, more explicitly, is inversely proportional to the slope of the crystal reactance curve shown in Fig. 119(b). The slope of this curve is a function of the difference between the resonant frequency f_r and the antiresonant frequency f_a. This frequency difference, in turn, is a function of the crystal capacitance ratio C_0/C_1, where C_0 and C_1 are the inherent shunt and series capacitances, respectively, of the crystal structure, as shown in Fig. 118.

The slope of the reactance curve is also a function of the total external crystal load capacitance C_L. As shown in Fig. 119(b), this slope decreases as the equivalent reactance increases (i.e., for smaller values of the capacitance C_L). Fig. 122 and Table XVII show trimming-range data for a typical

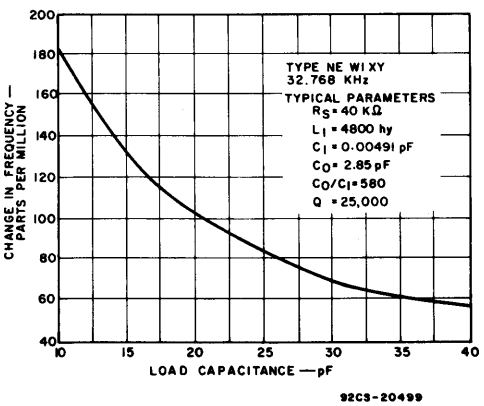


Fig. 122 – Frequency as a function of load capacitance for a typical 32-kHz crystal.

32.768-kHz crystal that has a capacitance ratio C_0/C_1 of 580. These data show that smaller values of load capacitance result in greater trimming-range capability.

Table XVII — Trimming Data for a Typical 32-kHz Quartz Oscillator Crystal

TRIM	LOAD CAPACITANCE, C_L			
	5 pF	11.5 pF	20 pF	32 pF
± 20 PPM	−0.45 pF +0.51	−1.6 pF +2.0	−3.7 pF +5.5	−8.0 pF +14.7
± 25 PPM	−.55 pF +.65	−1.9 pF +2.6	−4.5 pF +7.3	−9.4 pF +20.5
± 30 PPM	−0.66 pF +0.79	−2.3 pF +3.3	−5.2 pF +9.3	−10.7 pF +27.9

Temperature Stability

Another important oscillator consideration is temperature stability. Most crystals have a negative parabolic temperature coefficient. Fig. 123 shows a typical curve of the variation in crystal frequency as a function of temperature. The frequency of the total oscillator circuit also exhibits a similar temperature dependence. Temperature compensation of the over-all oscillator circuit can be achieved by use of a capacitor that has a positive parabolic temperature coefficient in the pi feedback network. For comparison, Fig. 123 shows a typical resultant curve for the over-all circuit.

The temperature characteristics of a crystal are determined to a large extent by the crystal cut. Popular low-frequency cuts include the NT and XY Bar. The XY Bar is the more popular of the two types because it can be made smaller for a given Q and is easier to trim. The disadvantage of a slightly lower shock resistance of XY-Bar crystals is compensated by the superior aging characteristics of this type.

AT-cut crystals, when used at frequencies greater than 1 MHz, are characterized by excellent temperature stability and ruggedness. Temperature characteristics for this type of crystal cut, as well as for the XY-Bar and NT types, are shown in Fig. 124.

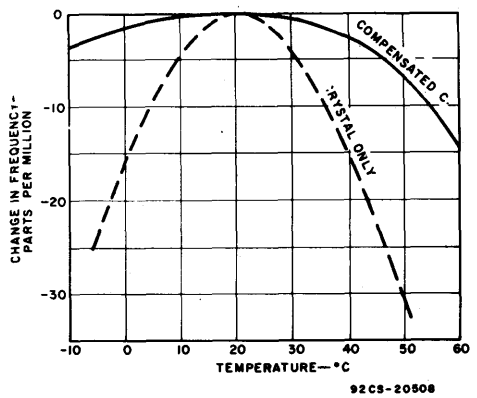


Fig. 123 — Effect of temperature on crystal frequency.

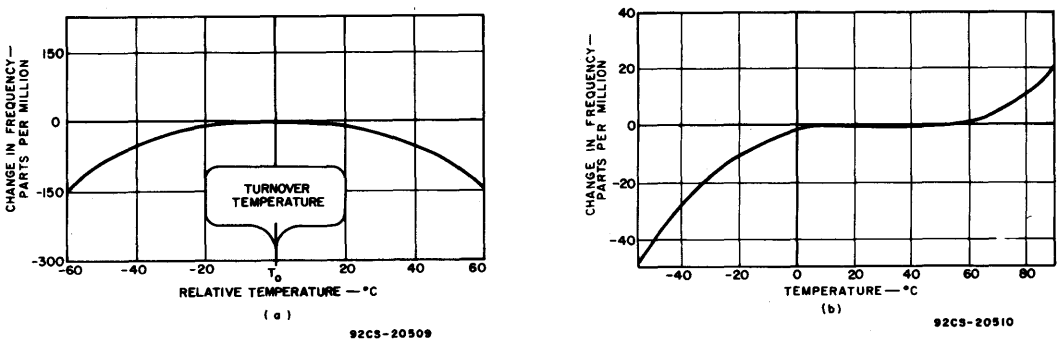


Fig. 124 — Frequency-temperature characteristics for various crystal cuts: (a) XY-Bar and NT cuts; (b) AT cut.

Crystal Dimensions

Size is also an important consideration in the design of oscillator crystals. The length of quartz required for any given cut is inversely proportional to the square root of frequency. Dimensions for a typical packaged 32-kHz XY-Bar crystal are 0.6 inch by 0.2 inch by 0.11 inch. The smallest XY-Bar crystals currently available have dimensions in the order of 0.53 inch by 0.2 inch by 0.11 inch. A 1-MHz AT-cut crystal is significantly larger; however, dimensions again decrease with frequency. Crystal manufacturers are currently working to develop wrist-watch-size-AT-cut crystals with the anticipation of circuit improvements that will allow low-current operation at high frequencies.

Crystal Shock Resistance and Aging Rate

A prime concern of the timing industry today is that of crystal shock resistance and aging. The aging of a crystal results primarily from aging of the mounting material rather than from aging of the quartz itself. Because the mounting material enters into the crystal equivalent circuit, the slowest aging rate results when the mount consists of the least amount of supporting material. However, this condition results in lower shock resistance, and an optimum tradeoff must be achieved.

At present, 32-kHz crystals can be made that can withstand a mechanical shock of about 1500 G's applied for 0.5 millisecond and that have aging rates that result in a frequency change of 2 to 5 parts per million for the first year and essentially no aging thereafter. Any mechanical or thermal shock, however, will interrupt the normal aging process. The aging rate of 2 to 5 parts per million presently appears acceptable to the timing industry, although shock resistances of 3,000 to 5,000 G's are desired. This shock level corresponds approximately to the shock experienced when a crystal is dropped from a height of one meter onto a hardwood floor.

PRACTICAL OSCILLATOR CIRCUITS

The basic amplifier, feedback-network, and crystal considerations discussed in the preceding pages can be combined in the design of COS/MOS oscillator circuits. In the circuits shown in Fig. 125, the crystal selected has an equivalent resistance R_e of 50 kilohms and is cut to operate at a frequency

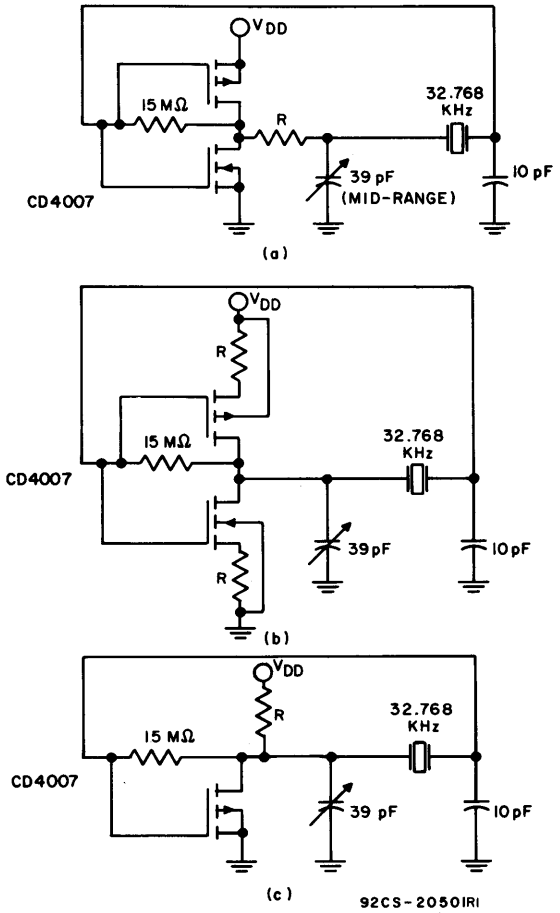


Fig. 125 – Typical COS/MOS crystal oscillator circuits.

of 32.768 kHz with a load capacitance C_L of 10 picofarads. The values of pi-feedback-network capacitors C_T and C_S can be calculated, as described previously, to be 43 and 13 picofarads, respectively. The value of the feedback-network resistance R can be calculated as follows:

$$R = \frac{(3X_e + 0.27R_e)(X_e - 0.8R_e)}{16R_e}$$

$$\cong 1 \text{ megohm}$$

This value is the maximum value of resistance allowed for a minimum feedback-network attenuation factor of 0.75, a value

selected on the basis of power and stability considerations. The calculated value of R includes any fixed resistance plus the amplifier output resistance. Because the output resistance is often appreciable and varies with supply voltage, transistor size, and threshold voltages, it is generally best to add resistance experimentally until the desired power consumption and frequency stability are reached. The effect of this resistance on operating current and frequency stability can be predicted from the data given in Table XVIII for the three COS/MOS crystal-oscillator circuits shown in Fig. 125. In each circuit, the pi-network capacitors C_T and C_S are 39 picofarads and 10 picofarads, respectively. These capacitances are slightly less than the calculated values because of stray and amplifier capacitances.

The circuit shown in Fig. 125(a) combines the amplifier and feedback circuits shown in Figs. 120 and 121. Although theory predicts that an increase in the values of the feedback-network resistor R will result in increased frequency stability, the circuit performance data given in Table XVIII show no significant improvement in this characteristic. This result indicates that the circuit instability can be attributed almost entirely to phase instabilities of the amplifier.

The assumption is verified by data taken from the circuits shown in Figs. 125(b) and 125(c), in which the required feedback-network resistance is incorporated into the amplifier as a fixed value. The resistors essentially fix the amplifier phase shift so that greater stability results. As the data show, use of these resistors also results in a decrease in the total current consumption. Because of the two fixed resistors, the circuit of Fig. 125 (b) shows the least current consumption and also the greatest stability.

As mentioned previously, the amplifier feedback resistor should not significantly

Table XVIII – Typical Oscillator Data

Circuit Fig. 125	Value of R (Ω)	V_{DD} (Volts)	Current (μA)	Change in Frequency V_{DD}=1.45 V to 1.6 V (Parts per million)
(a)	0	1.60	4.0	2.8
"	0	1.45	3.1	
"	100K	1.60	3.1	2.6
"	"	1.45	2.4	
"	200K	1.60	2.9	2.6
"	"	1.45	2.1	
(b)	100K	1.60	2.3	0.3
"	"	1.45	2.0	
"	"	1.1	1.5	
"	150K	1.60	1.8	0.2
"	"	1.45	1.6	
"	"	1.1	0.95	
(c)	200K	1.60	5.0	0.6
"	"	1.45	4.4	
"	300K	1.60	3.5	0.5
"	"	1.45	3.0	

load the crystal feedback network. The resistor value at which loading begins to occur can be determined from a curve of circuit operating frequency as a function of feedback resistance. Fig. 126 shows such a curve for the circuit shown in Fig. 125(b). This curve indicates that 15 megohms is a suitable value for the feedback resistor.

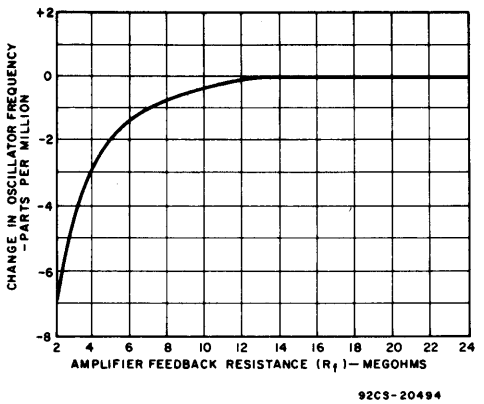


Fig. 126 – Oscillator frequency as a function of amplifier feedback resistance.

Operating Frequencies

A wide range of frequencies is attainable with COS/MOS crystal oscillator circuits. Frequencies up to about 10 MHz are possible at a V_{DD} of 15 volts. Beyond 10 MHz, the phase shift becomes too large, and stability decreases accordingly. The lowest frequency of operation depends only on the equivalent resistance of the crystal. Values of R_s and R_e increase rapidly at the lower frequencies and require amplifiers with high input impedance to minimize the attenuation across the feedback network.

Because COS/MOS amplifiers have high input impedances (about 10^{12} ohms), much lower frequencies are possible in COS/MOS antiresonant oscillator circuits than in bipolar antiresonant circuits. Frequencies down to 2 kHz can be achieved by using the three inverters in one CD4007 package connected in parallel to provide the greater current drive required by the crystal at this frequency.

Frequencies lower than 2 kHz are easily obtained by counting down the oscillator frequency. For example, a 16.384-kHz oscillator can be used to drive a 14-stage binary counter, with the last stage counting at one pulse per second. Fig. 127 shows such a circuit using the CD4060 COS/MOS integrated circuit, which consists of an oscillator section and 14 binary counter stages.

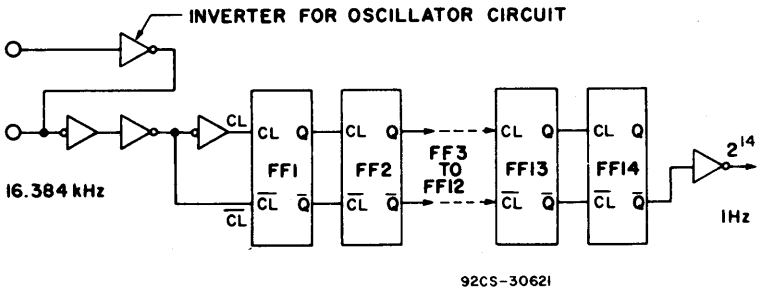


Fig. 127 – Functional diagram of the CD4060 COS/MOS oscillator interconnected with a 14-stage binary counter.

VIII. Shift Registers and Counters

COS/MOS shift registers generally use the basic static master-slave flip-flop circuit configuration described in Chapter II and reproduced in Fig. 128. The logic level present at the D(Data) input is transferred to the Q output during either the positive- or negative-going transition of the clock, depending on the specific circuit type. Set and reset functions may be included, again depending on circuit type; if they are included, each function is accomplished by a high level at the respective input. In a serial shift register, the Q output of one stage becomes the D input of the following stage.

Ripple-carry binary counters are similar to shift registers except that the D input to each stage is connected to the Q output of the same stage, so that is complements the stage at the clock transistion. The Q and Q outputs of one stage become the Clock and Clock inputs of the following stage.

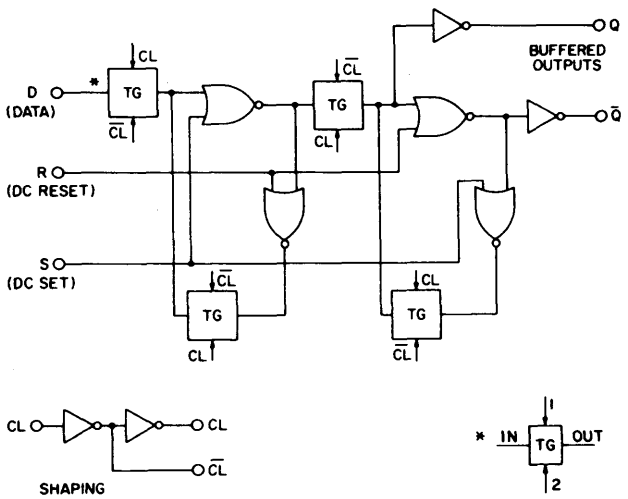
In a synchronous binary counter, a common clock is used for all stages; the Q output is returned to the D input, as in the ripple counter.

COS/MOS shift registers and counters are available in a number of different integrated-circuit configurations that afford the designer considerable versatility in implementing system designs. The brief descriptions and diagrams shown in this chapter for a wide variety of shift registers and counters can serve as a selection guide to RCA types.

STATIC SHIFT REGISTERS

Dual 4-Stage Static Shift Register with Serial Input/Parallel Output

The CD4015 consists of two identical, independent, 4-stage serial-input/parallel-



TRUTH TABLE

CL	D	R	S	Q	$\bar{Q}$
↓	0	0	0	0	1
↓	1	0	0	1	0
↑	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	*	*

(NO CHANGE)

* - INVALID CONDITION
▲ - LEVEL CHANGE
X - DON'T CARE CASE

INPUT TO OUTPUT IS A BIDIRECTIONAL SHORT CIRCUIT WHEN CONTROL-INPUT 1 IS LOW AND CONTROL-INPUT 2 IS HIGH; AN OPEN CIRCUIT WHEN CONTROL-INPUT 1 IS HIGH AND CONTROL-INPUT 2 IS LOW.

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Fig. 128 – Basic master-slave flip-flop circuit used in COS/MOS shift registers and counters.

output registers, as shown in Fig. 129. Each register has independent clock and reset inputs, as well as a single serial data input. Q outputs are available from each of the four stages on both registers. All register stages are D-type master-slave flip-flops.

The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. The register can be expanded to eight stages using one CD4015 package, or to more than eight stages using additional CD4015 packages.

18-Stage Static Shift Register

The CD4006, shown in Fig. 130, consists of 4 separate shift-register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on

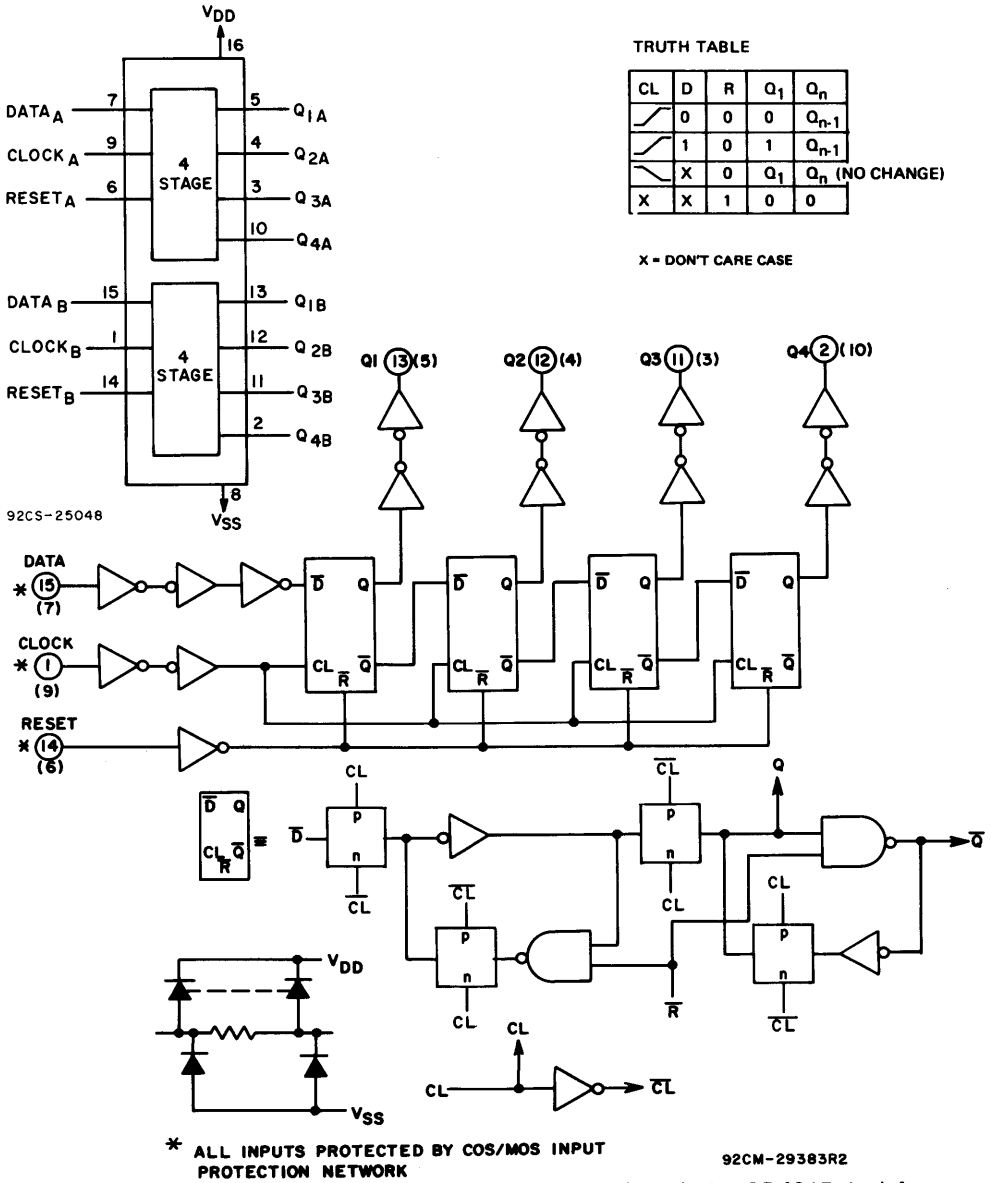


Fig. 129 – Functional diagram, logic diagram, and truth table for CD4015 dual 4-stage static shift register.

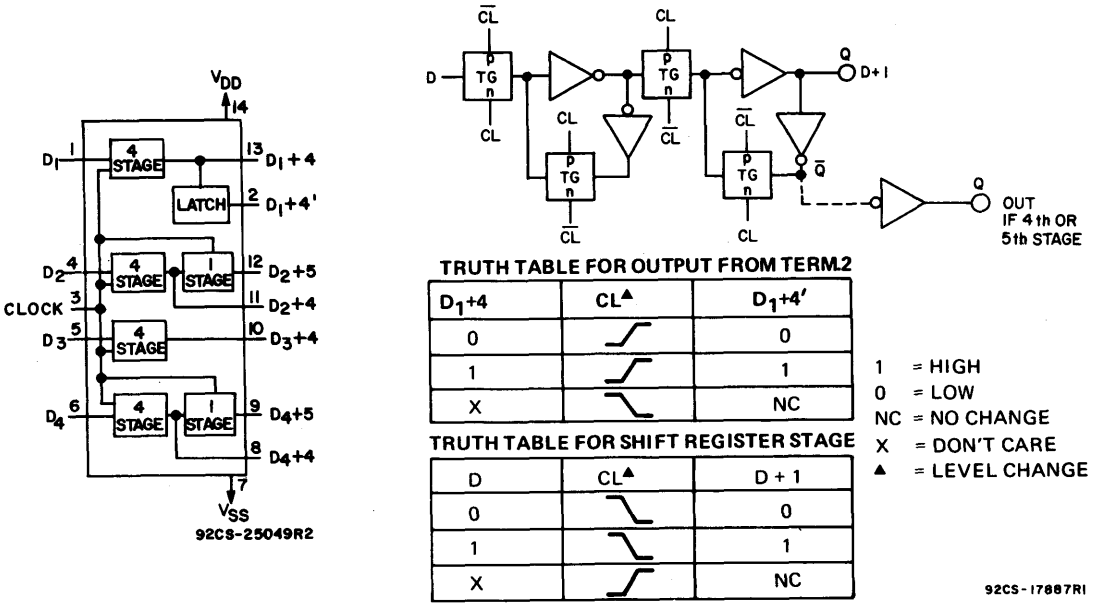


Fig. 130 – Functional diagram, logic diagram, and truth table for CD4006 18-stage static shift register.

negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, and 18 stages can be implemented using one CD4006 package. Longer shift-register sections can be assembled by use of more than one CD4006.

64-Stage Static Shift Register

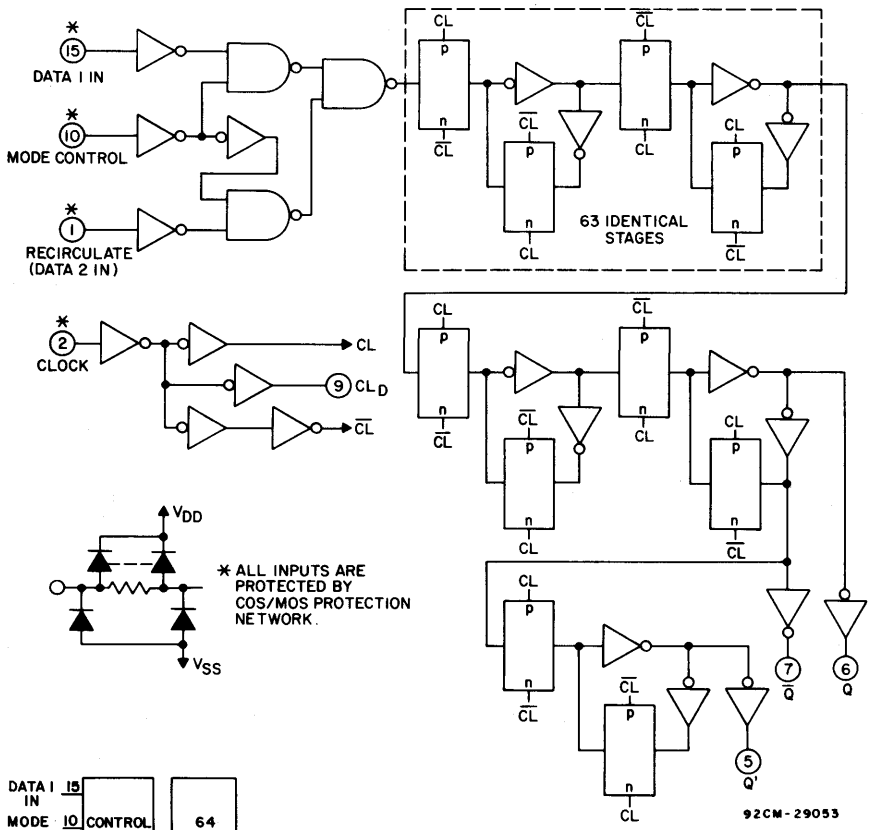
The CD4031 is a 64-stage static shift register in which each stage is a D-type master-slave flip-flop. The functional diagram, logic diagram, and truth table for the CD4031 are shown in Fig. 131.

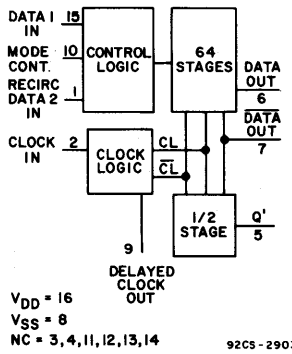
The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 4 MHz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031 has a mode control input that, when in the high state, allows operation in the recirculating mode. Register packages can be cascaded and the clock lines driven directly for high-speed operation, as shown in Fig. 132. Alternatively, a delayed clock output (CL_D) is provided that makes it possible to cascade register packages while allowing reduced clock drive fanout and transition-time requirements, as shown in Fig. 133.

Data (Q) and Data ($\overline{Q}$) outputs are provided from the 64th register stage. The Data ($\overline{Q}$) output is capable of driving one TTL or DTL load.

8-Stage Static Shift Register with Synchronous Parallel or Serial Input/Serial Output

Fig. 134 shows the functional diagram, logic diagram, and truth table for the CD4014 8-stage parallel or serial-input/serial-output register. This circuit has common clock and parallel/serial control inputs, a single serial data input, and individual parallel "jam" inputs to each register stage. Each stage is a D-type master-slave flip-flop. Q outputs are available from stages 6 and 7, as well as from stage 8. Parallel or serial entry is made into the register synchronous with the positive clock-line transition and under control of the parallel/serial control input.





INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE I
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

TYPICAL STAGE TRUTH TABLE

Data	CL	Data + 1
0	⌐	0
1	⌐	1
X	⌐	NC

TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

Data + 64	CL	Data + 64½
0	⌐	0
1	⌐	1
X	⌐	NC

1 = HIGH LEVEL 0 = LOW LEVEL NC = NO CHANGE
X = DON'T CARE

Fig. 131 — Functional diagram, logic diagram, and truth table for CD4031 64-stage static shift register.

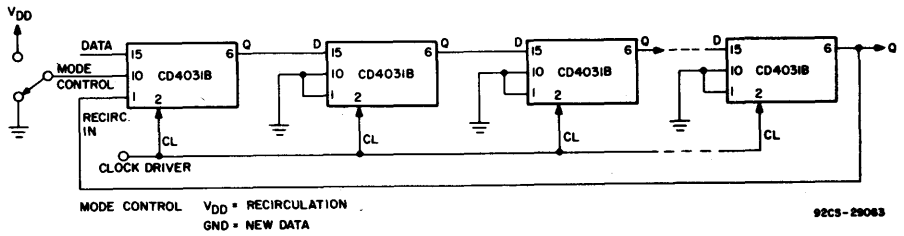


Fig. 132 – Cascading of CD4031 devices using direct clocking for high-speed operation.

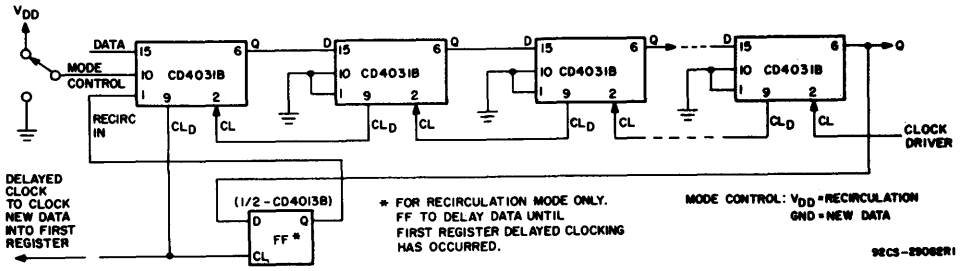


Fig. 133 – Cascading of CD4031 devices using delayed clocking for reduced clock-drive requirements.

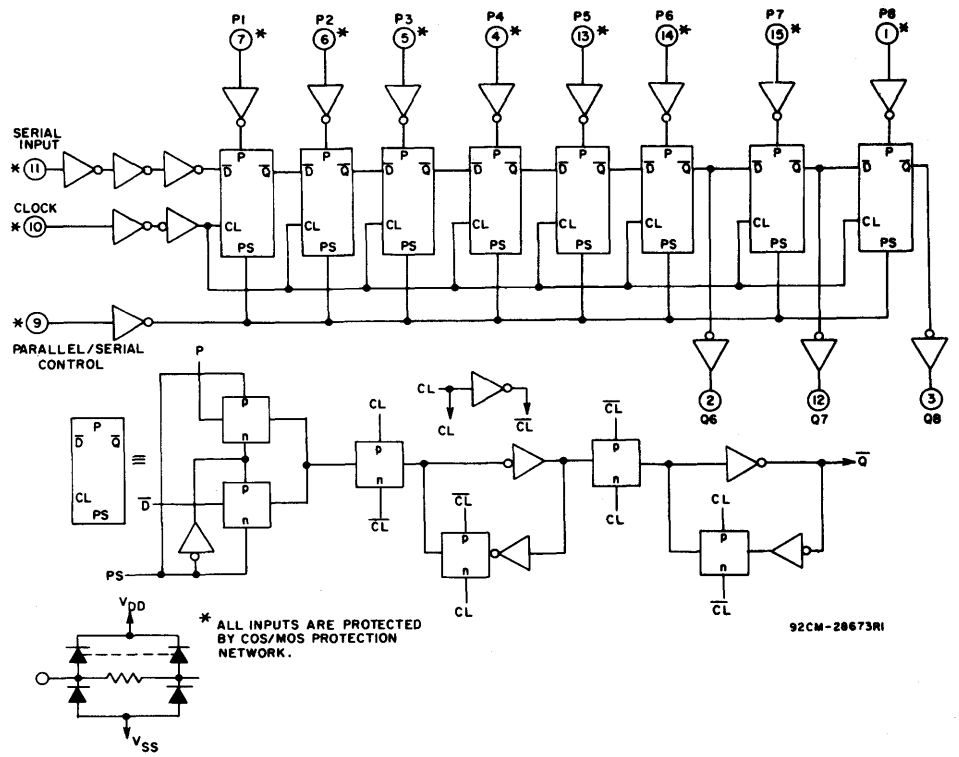
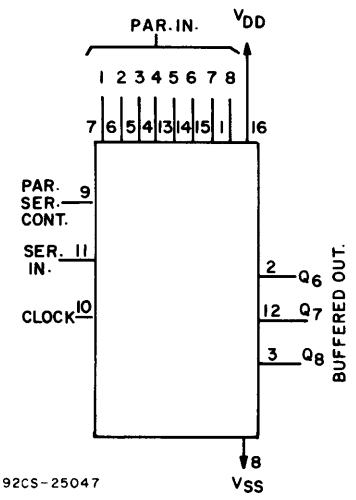


Fig. 134(a) – Logic diagram for CD4014 8-stage static shift register.



CL ▲	SER. IN	PAR SER CONTROL	PI-1	PI-n	Q_1 (INTER-NAL)	Q_n	
⟋	X	1	0	0	0	0	
⟋	X	1	1	0	1	0	
⟋	X	1	0	1	0	1	
⟋	X	1	1	1	1	1	
⟋	0	0	X	X	0	Q_n-1	
⟋	1	0	X	X	1	Q_n-1	
⟍	X	X	X	X	Q_1	Q_n	NC

X = DON'T CARE CASE ▲ = LEVEL CHANGE
NC = NO CHANGE

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Fig. 134(b) — Functional diagram and truth table for CD4014 8-stage static shift register.

8-Stage Static Shift Register with Asynchronous Parallel or Synchronous Serial Input/Serial Output

The CD4021, shown in Fig. 135, is an 8-stage parallel- or serial-input/serial-output shift register that has common clock and parallel/serial control inputs, a single serial data input, and individual parallel "jam" inputs to each register stage. Each register stage is a D-type master-slave flip-flop. Q outputs are available from the sixth, seventh, and eighth stages.

When the parallel/serial control input is low, data are serially shifted into the 8-stage register synchronously with the positive-

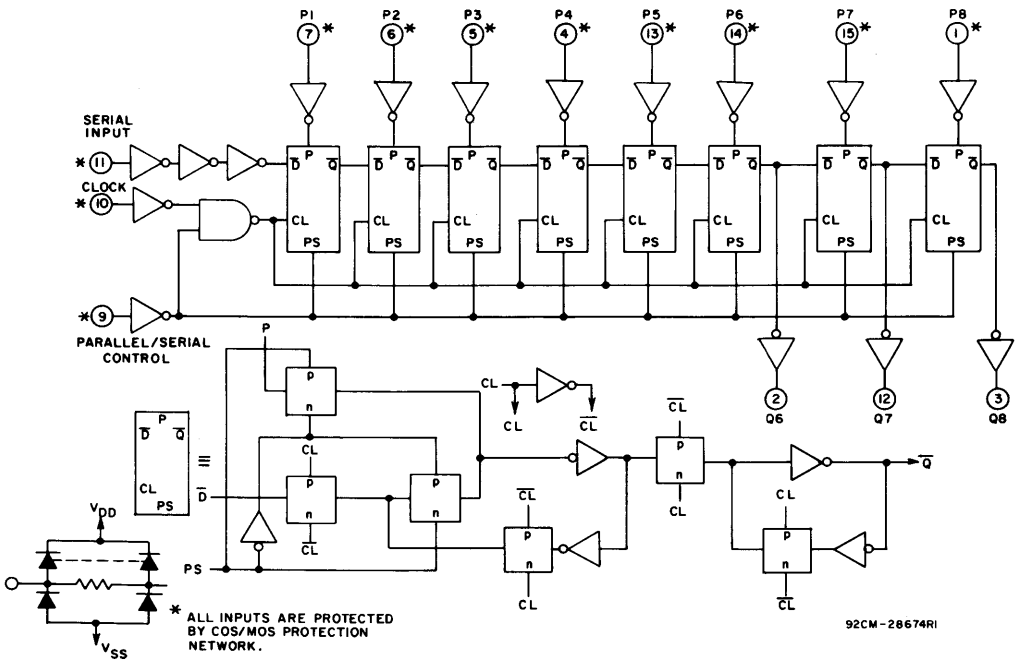
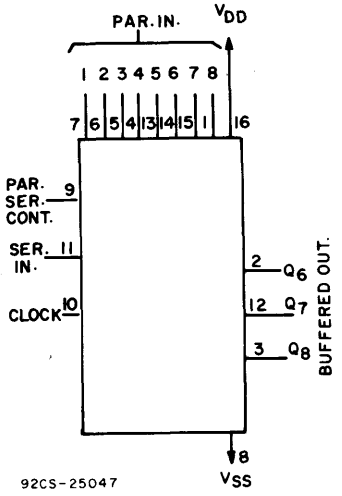


Fig. 135(a) — Logic diagram for CD4021 8-stage static shift register.



CL ▲	SER. IN	PAR SER CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n
↗	X	1	0	0	0	0
↗	X	1	0	1	0	1
↗	X	1	1	0	1	0
↗	X	1	1	1	1	1
↗	0	0	X	X	0	Q_n-1
↗	1	0	X	X	1	Q_n-1
↘	X	0	X	X	Q_1	Q_n NC

X = DON'T CARE CASE ▲ = LEVEL CHANGE
NC = NO CHANGE

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Fig. 135(b) — Functional diagram and truth table for CD4021 8-stage static shift register.

going transition of the clock pulse. When the parallel/serial control input is high, data are jammed into the 8-stage register by means of the parallel input lines asynchronously with the clock line.

Register expansion is possible using additional CD4021 packages.

4-Stage Parallel-In/Parallel-Out Shift Register with J-K Serial Inputs and True/Complement Outputs

Fig. 136 shows the functional diagram, logic diagram, and truth table for the CD4035. This four-stage clocked-signal serial register has provision for synchronous parallel inputs to each stage and serial inputs to the first stage by means of J-K logic. When the register is in the serial mode (parallel/serial control low), stages 2, 3, and 4 are coupled in a serial D flip-flop configuration. Parallel entry by means of the D line of each register stage is permitted only when the parallel/serial control is high. In the parallel or serial mode, information is transferred on positive clock transitions.

When the true/complement control is high, the true contents of the register are available at the output terminals. When the true/complement control is low, the outputs are the complements of the data in the register. The true/complement control functions asynchronously with respect to the clock signal.

J-K input logic is provided on the first-stage serial input to minimize logic requirements, particularly in counting and sequence-generation applications. With J-K inputs connected together, the first stage becomes a D flip-flop. An asynchronous common reset is also provided.

8-Stage Bidirectional Bus Register with Parallel or Serial Input/Parallel Output

The CD4034 is a static eight-stage parallel- or serial-input/parallel-output register, as shown in Fig. 137. It can be used to (1) bidirectionally transfer parallel information between two buses, (2) convert serial data to parallel form and direct the parallel data to either of two buses, (3) store or recirculate parallel data, or (4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase clock (CL), A-data enable (AE), asynchronous/synchronous (A/S), A-bus-to-B-bus/B-bus-to-A-bus (A/B), and parallel/serial (P/S). The steering logic diagram for the CD4034 is shown in Fig. 138.

Data inputs include 16 bidirectional parallel data lines, of which the eight A data lines are inputs or outputs and the eight B data lines are outputs or inputs, depending on the signal level on the A/B input. An input for serial data is also provided.

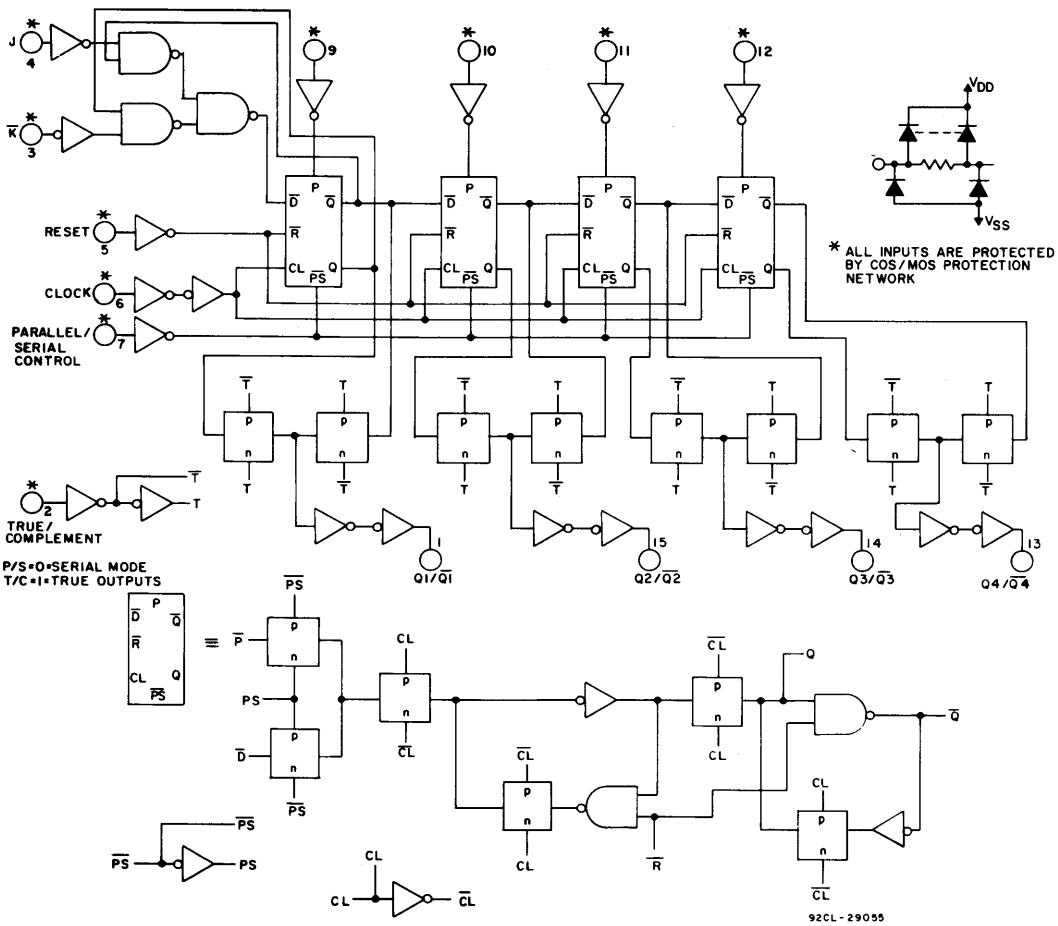
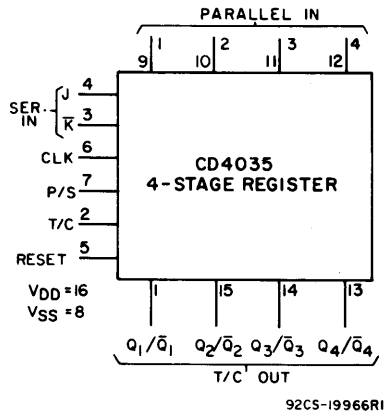


Fig. 136(a) – Logic diagram for CD4035 4-stage static shift register.



FIRST STAGE TRUTH TABLE

	t_{n-1} (INPUTS)				t_n (OUTPUTS)
CL	J	$\overline{K}$	R	Q_{n-1}	Q_n
↑	0	X	0	0	0
↑	1	X	0	0	1
↑	X	0	0	1	0
↑	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
↑	X	1	0	1	1
↓	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Fig. 136(b) – Functional diagram and truth table for CD4035 4-stage static shift register.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous data transfer from master to slave. The logic diagram for one of the eight identical register stages is shown in Fig. 139. Isolation from external noise and the effects of loading is provided by output buffering.

4-Bit Bidirectional Universal Shift Register

Fig. 140 shows the functional diagram and truth table for the CD40194. This universal shift register features parallel inputs, parallel outputs, shift-right and shift-left serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 high), data are loaded into the associated flip-flop and

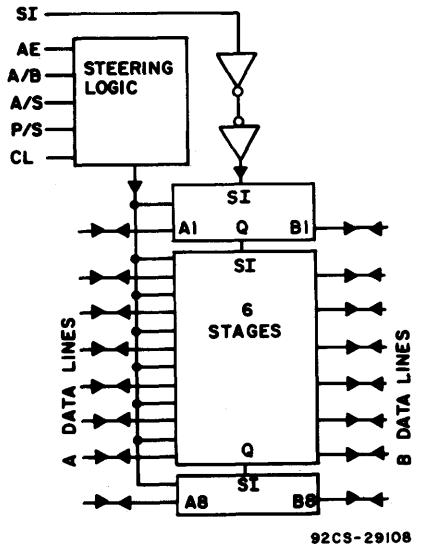


Fig. 137 – Functional diagram for CD4034 8-stage static bidirectional bus register.

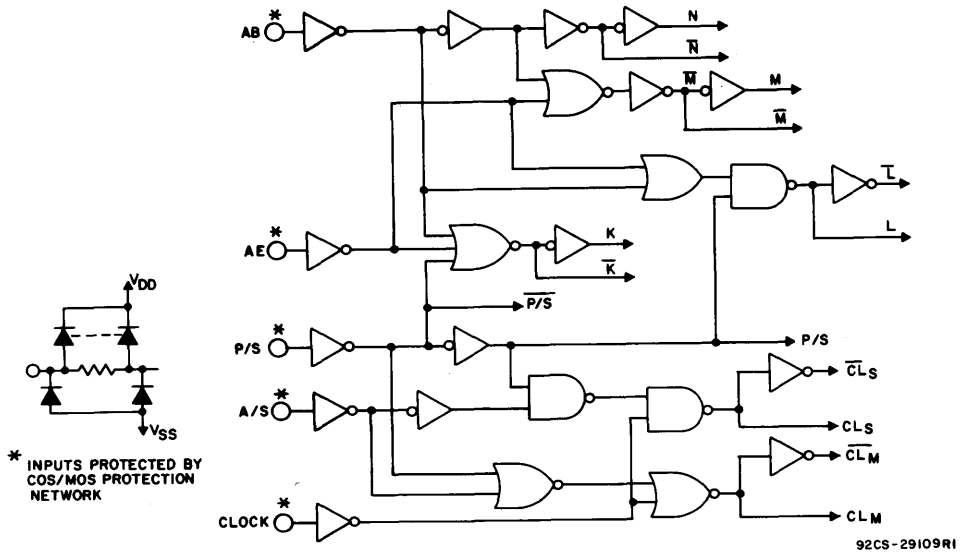


Fig. 138 – Steering logic diagram for CD4034.

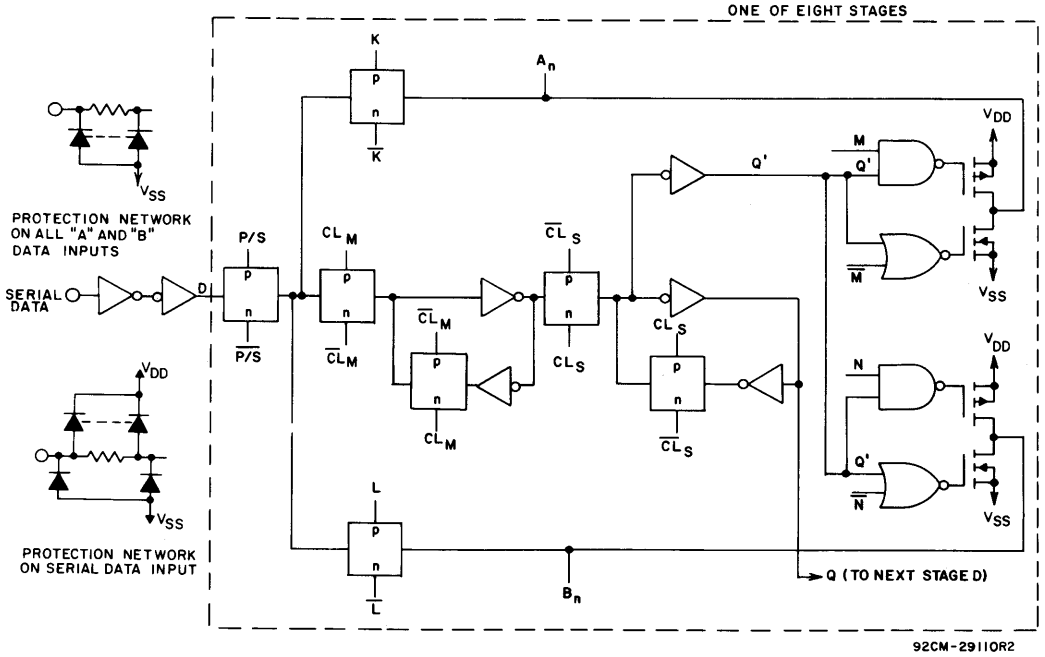
appear at the output after the positive transition of the clock input. During loading serial data flow is inhibited.

Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the shift-right and shift-left serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. The mode controls should be changed only when the clock input is low. When the reset input is low, it resets all stages and forces all outputs low.

4-Bit Bidirectional Universal Register with 3-State Output

The CD40104, shown in Fig. 141, is a universal register featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs, and a high-impedance third output state that allows the device to be used in bus-organized systems.

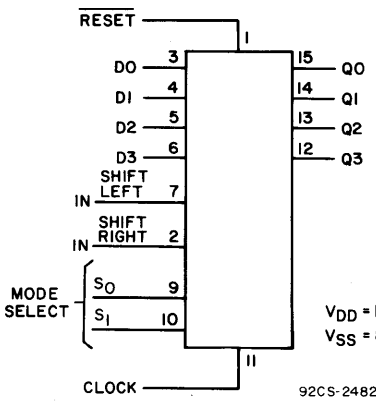
As in the CD40194, data are loaded into the associated flip-flop in the parallel-load



INPUTS			OUTPUT
$\overline{CL}_M$	$\overline{CL}_S$	D	Q
↓	↓	0	0
↑	↑	0	0
↓	↑	0	INVALID CONDITION
↑	↑	X	0
↓	↓	1	1
↑	↓	1	1
↓	↑	1	INVALID CONDITION

1 = High Level 0 = Low Level X = Don't Care

Fig. 139 – Logic diagram and truth table for one of eight identical register stages in CD4034 shift register.



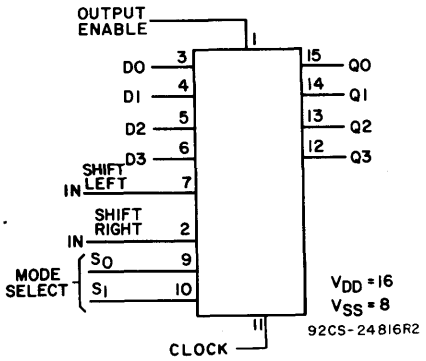
CL	S0	S1	$\overline{RESET}$	ACTION
X	0	0	1	Do-Nothing
↑	1	0	1	Shift Right (Q0 toward Q3)
↑	0	1	1	Shift Left (Q3 toward Q0)
↑	1	1	1	Parallel Load
X	X	X	0	Reset

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE

Fig. 140 – Functional diagram and truth table for CD40194 4-bit universal shift register.

mode and appear at the output after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right and shift-left serial inputs, respectively.

synchronously with the positive clock edge, provided the left/right control is at a low level, the recirculate control is at a high level, and the clock inhibit is low. If the left/right control is at a high level and the recirculate control is also high, data at the shift-left input is transferred into the 32nd register



CONTROL TRUTH TABLE

CLOCK▲	MODE S_0	SELECT S_1	OUTPUT ENABLE	ACTION
⌐¬	0	0	1	Reset
⌐¬	1	0	1	Shift right (Q_0 toward Q_3)
⌐¬	0	1	1	Shift left (Q_3 toward Q_0)
⌐¬	1	1	1	Parallel load
X	X	X	0	Outputs assume high impedance

1 = High level
0 = Low level

X = Don't care
▲ = Level change

Fig. 141 – Functional diagram and truth table for CD40104 4-bit universal register with 3-state output.

Clearing the register is accomplished by setting both mode controls low and clocking the register. The mode controls should be changed only when the clock input is low. When the output-enable input is low, all outputs assume the high-impedance state.

32-Stage Left/Right Static Shift Register

Fig. 142 shows the functional diagram for the CD40100, a static shift register containing 32 D-type master-slave flip-flops. The logic diagram and truth tables are shown in Fig. 143.

The data present at the shift-right input are transferred into the first register stage

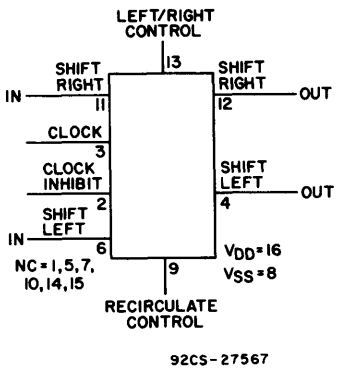


Fig. 142 – Functional diagram for CD40100 32-stage left-right static shift register.

stage synchronously with the positive clock transition, provided the clock inhibit is low.

Data are shifted one stage left or one stage right (depending on the state of the left/right control) synchronously with the positive clock edge. Data clocked into the first or 32nd register stage are available at the appropriate output on the next negative clock transition. No shifting occurs on the positive clock edge if the clock inhibit line is at a high level. With the recirculate control low, data are shifted from the 32nd stage into the first stage when the left/right control is low and from the first stage to the 32nd stage when the left/right control is high.

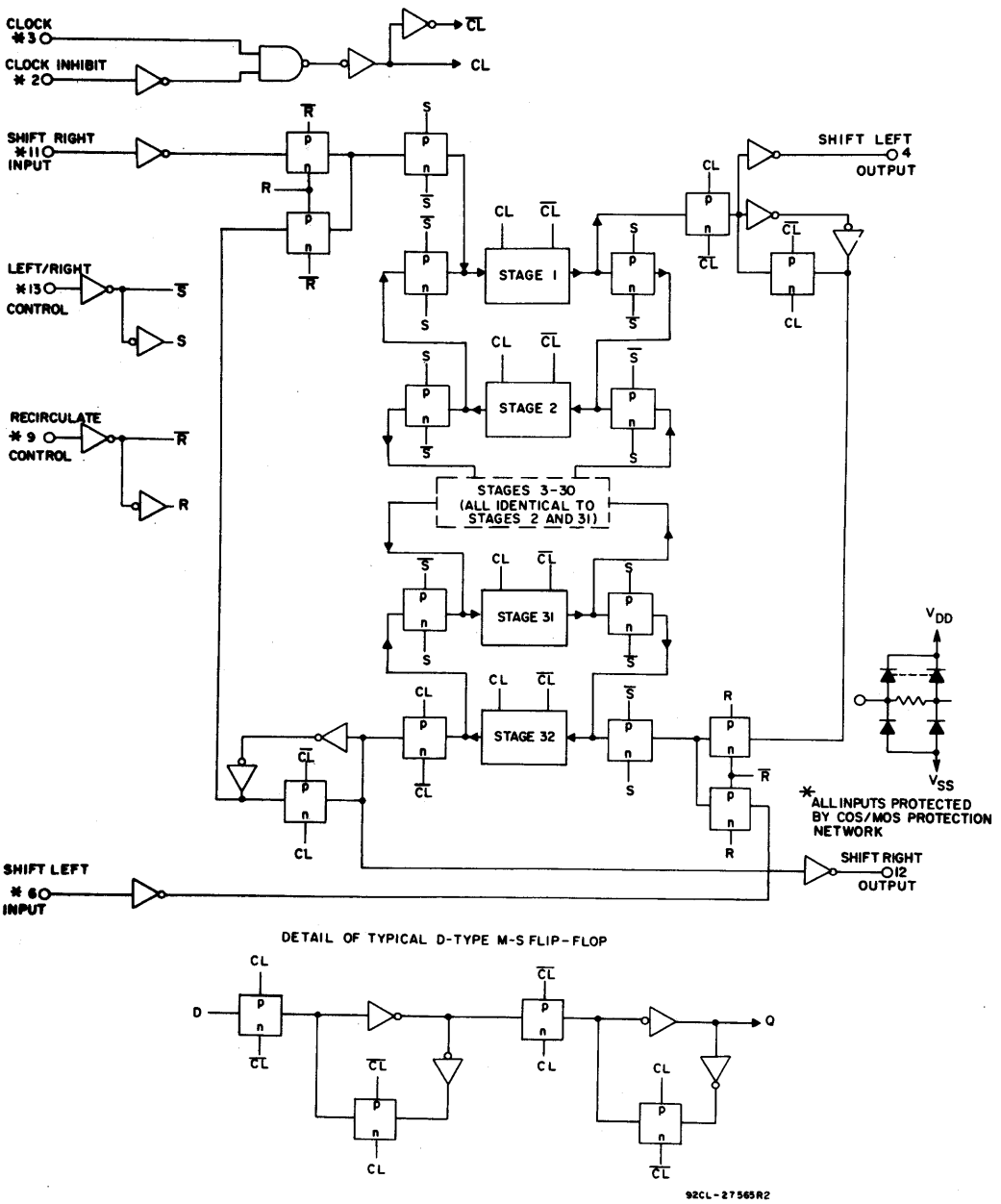


Fig. 143(a) — Logic diagram for CD40100 shift register.

CONTROL TRUTH TABLE

LEFT/RIGHT CONTROL	CLOCK INHIBIT	RECIRCULATE CONTROL	ACTION	INPUT BIT ORIGIN
1	0	1	Shift left	Shift left input
1	0	0	Shift left	Stage 1
0	0	1	Shift right	Shift right input
0	0	0	Shift right	Stage 32
X	1	X	No shift	–

DATA TRANSFER TABLE*

INITIAL STATE			CLOCK	RESULTING STATE	
DATA INPUT	CLOCK INHIBIT	INTERNAL STAGE	LEVEL CHANGE	INTERNAL STAGE Q	OUTPUT
0	0	X	⌐	0	NC
X	0	0	¬	NC	0
1	0	X	⌐	1	NC
X	0	1	¬	NC	1
X	1	1	X	NC	NC

0 = Low level 1 = High level X = Don't care NC = No change

* For Shift-Right Mode
Data Input = SHIFT-RIGHT INPUT (Term. 11)
Internal Stage = Stage 1 (Q_1)
Output = SHIFT-LEFT OUTPUT (Term. 4)

For Shift-Left Mode
Data Input = SHIFT-LEFT INPUT (Term. 6)
Internal Stage = Stage 32 (Q_{32})
Output = SHIFT-RIGHT OUTPUT (Term. 12)

Fig. 143(b) – Truth tables for CD40100 shift register.

8-Stage Shift-and-Store Bus Register

The CD4094 8-stage serial shift register, shown in Fig. 144, has a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data are shifted on positive clock transitions. The data in each shift-register stage are transferred to the storage register when the strobe input is high. Data in the storage register appear at the outputs whenever the output-enable signal is high.

Two serial outputs are available for cascading a number of CD4094 devices. Data are available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q_S terminal on the next negative clock edge, provides a means for cascading CD4094 devices when the clock rise time is slow.

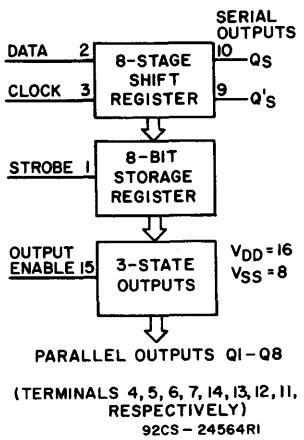


Fig. 144(a) – Functional diagram for CD4094 8-stage shift-and-store bus register.

DYNAMIC SHIFT REGISTERS

Fig. 145 shows the functional and logic diagrams for the CD4062 200-stage dynamic shift register, which has provision for either single- or two-phase clock input signals. Single-phase-clocked operation is intended

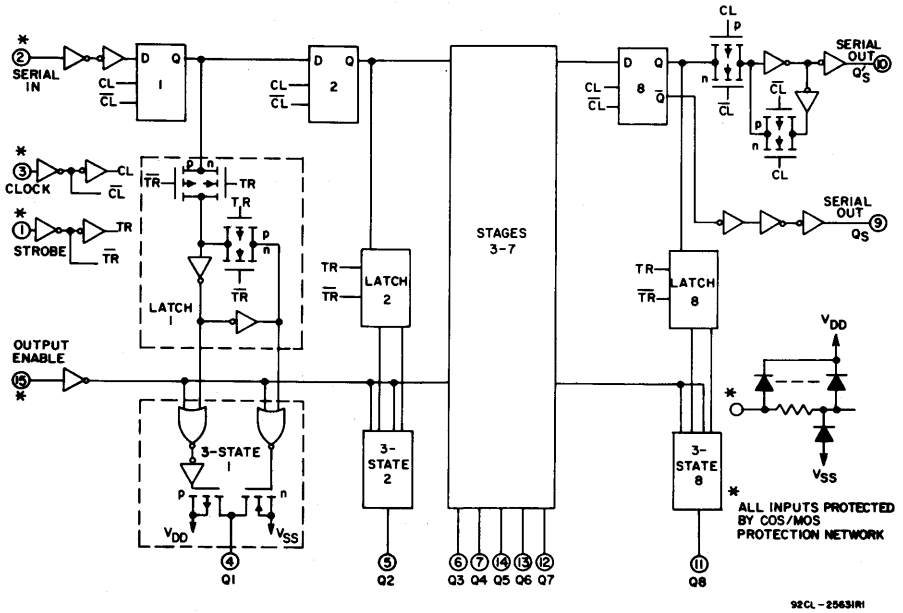


Fig. 144(b) – Logic diagram for CD4094 8-stage shift-and-store bus register.

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
⎍	0	X	X	OC	OC	Q7	NC
⎎	0	X	X	OC	OC	NC	Q7
⎍	1	0	X	NC	NC	Q7	NC
⎍	1	1	0	0	Q_{N-1}	Q7	NC
⎍	1	1	1	1	Q_{N-1}	Q7	NC
⎎	1	1	1	NC	NC	NC	Q7

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit

Logic 1 ≡ High
Logic 0 ≡ Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

Fig. 144(c) – Truth table for CD4094 8-stage shift-and-store bus register.

for low-power, low-clock-line-capacitance requirements. Single-phase clocking is specified for medium-speed operation (frequencies less than 1 MHz) at supply voltages up to 10 volts. Clock input capacitance is extremely low (less than 5 picofarads), and clock rise and fall times are non-critical. The clock-mode signal (CM) must be low for single-phase operation.

Two-phase clock-input signals may be used for high-speed operation (up to 5 MHz) or to further reduce clock rise- and fall-time requirements at low speeds. Two-phase operation is specified for supply voltages up to 15 volts. Clock input capacitance is only 50 picofarads per phase. The clock-mode signal (CM) must be high for two-phase operation. The single-phase-clock input has an internal pull-down device which is activated when CM is high and may be left unconnected in two-phase operation.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition for single-phase operation, and at the positive-going transition of CL_1 for two-phase operation.

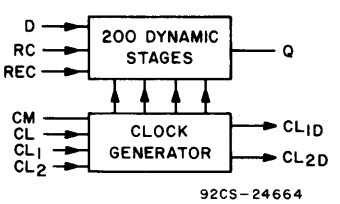


Fig. 145(a) – Functional diagram for the CD4062 200-stage dynamic shift register.

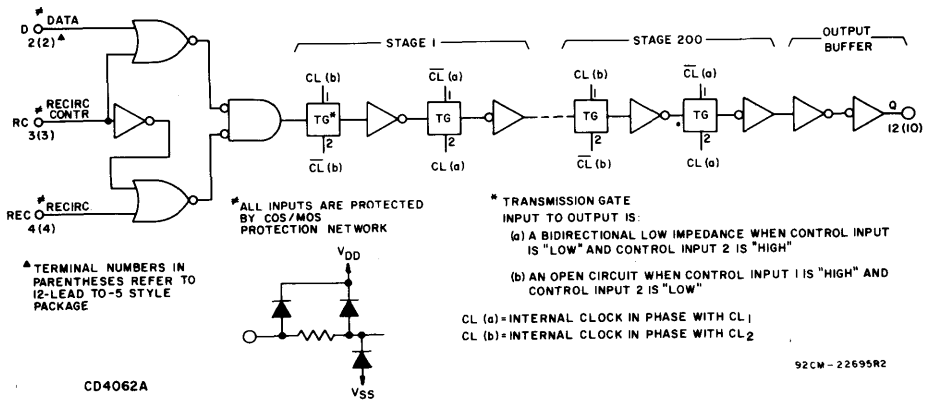


Fig. 145(b) – Logic diagram for the CD4062 200-stage dynamic shift register.

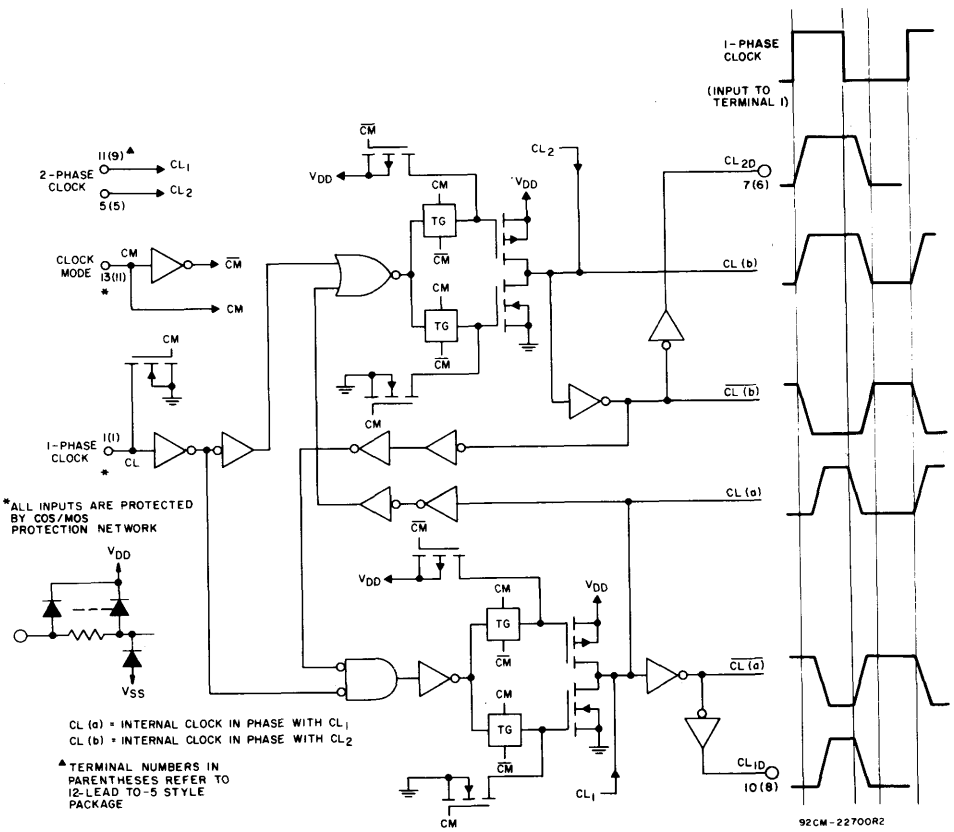


Fig. 145(c) – Clock circuit logic diagram for CD4062 200-stage dynamic shift register.

STORAGE REGISTERS

8-Bit Addressable Latch with Serial Input/Parallel Output

The CD4099 8-bit addressable latch, shown in Fig. 146, is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of binary inputs A0, A1, A2) and when the write-disable input is at a low level. When the write-disable input is high, data entry is inhibited; however, all eight outputs can be continuously read independent of write-disable and address inputs.

A master reset input is available, which resets all bits to a logic "0" level when the reset and write-disable inputs are at a high level. When the reset input is at a high level and the write-disable input is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

4-Bit D-Type Static Register with 3-State Outputs

Fig. 147 shows the functional and logic diagrams and truth table for the CD4076, a four-bit register consisting of D-type flip-flops that feature three-state outputs. Data-disable inputs are provided to control the entry of data into the flip-flops. When both data-disable inputs are low, data at the D

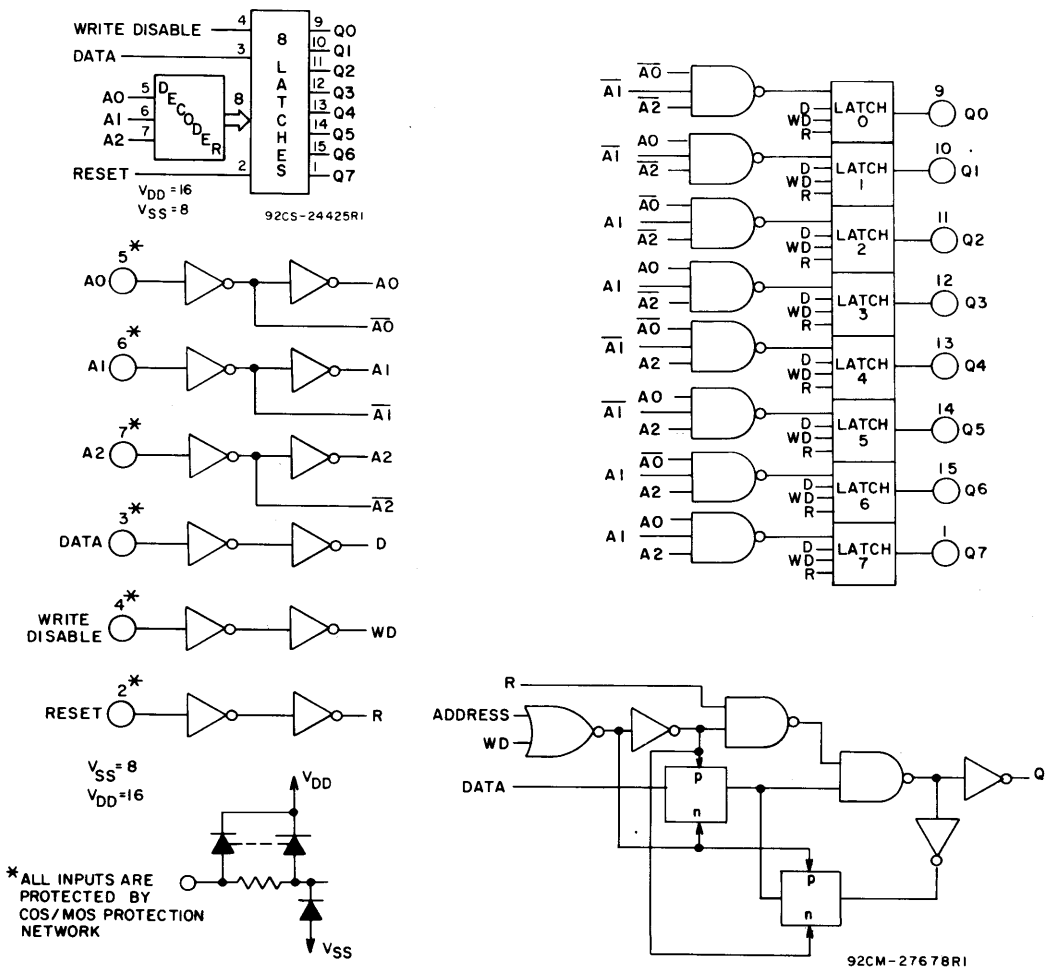


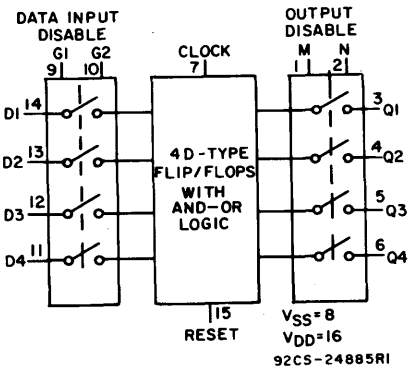
Fig. 146 – Functional and logic diagrams for CD4099 8-bit addressable latch.

inputs is loaded into the respective flip-flops on the next positive transition of the clock input.

Output-disable inputs are also provided. When the output-disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either output-disable input and present a high impedance.

4 X 4 Multiport Register with One Input and Two Output Buses (3-State)

The CD40208 is a multiport register containing four 4-bit registers, a write address decoder, two separate read address decoders, and two 3-state output buses, as shown in Fig. 148. The high-impedance third state



Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	⌐	1	X	X	Q	NC
0	⌐	X	1	X	Q	NC
0	⌐	0	0	1	1	
0	⌐	0	0	0	0	
0	1	X	X	X	Q	NC
0	⌙	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

1 ≡ High Level
0 ≡ Low Level
X = Don't Care
NC = No Change

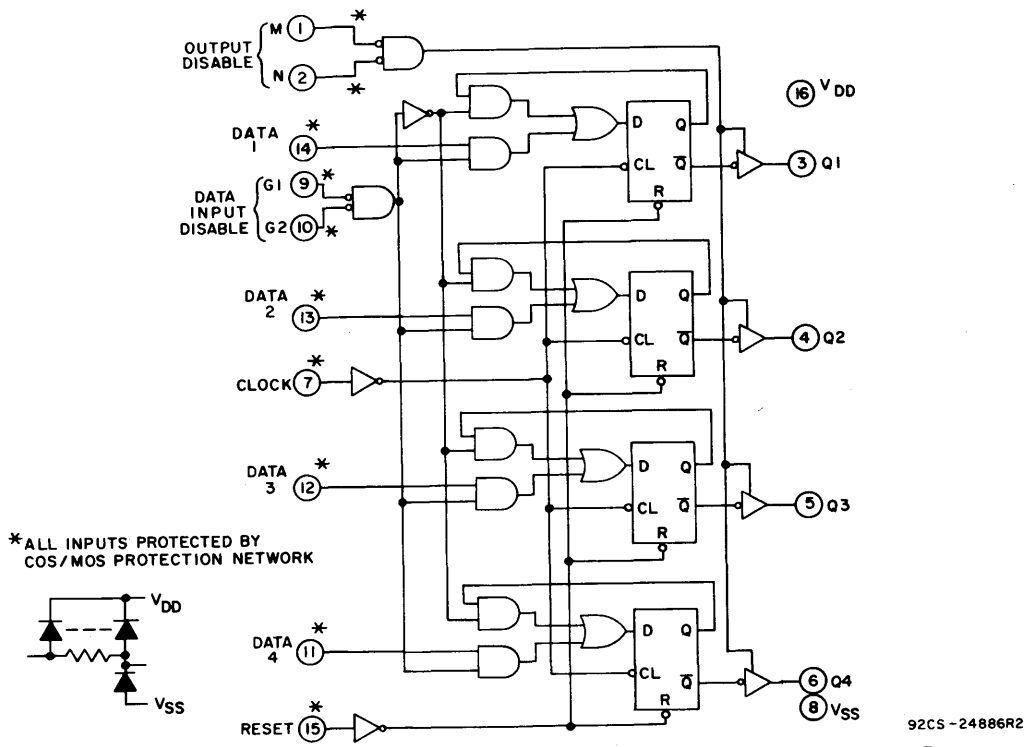


Fig. 147 — Functional and logic diagrams and truth table for the CD4076 4-bit D-type register with 3-state outputs.

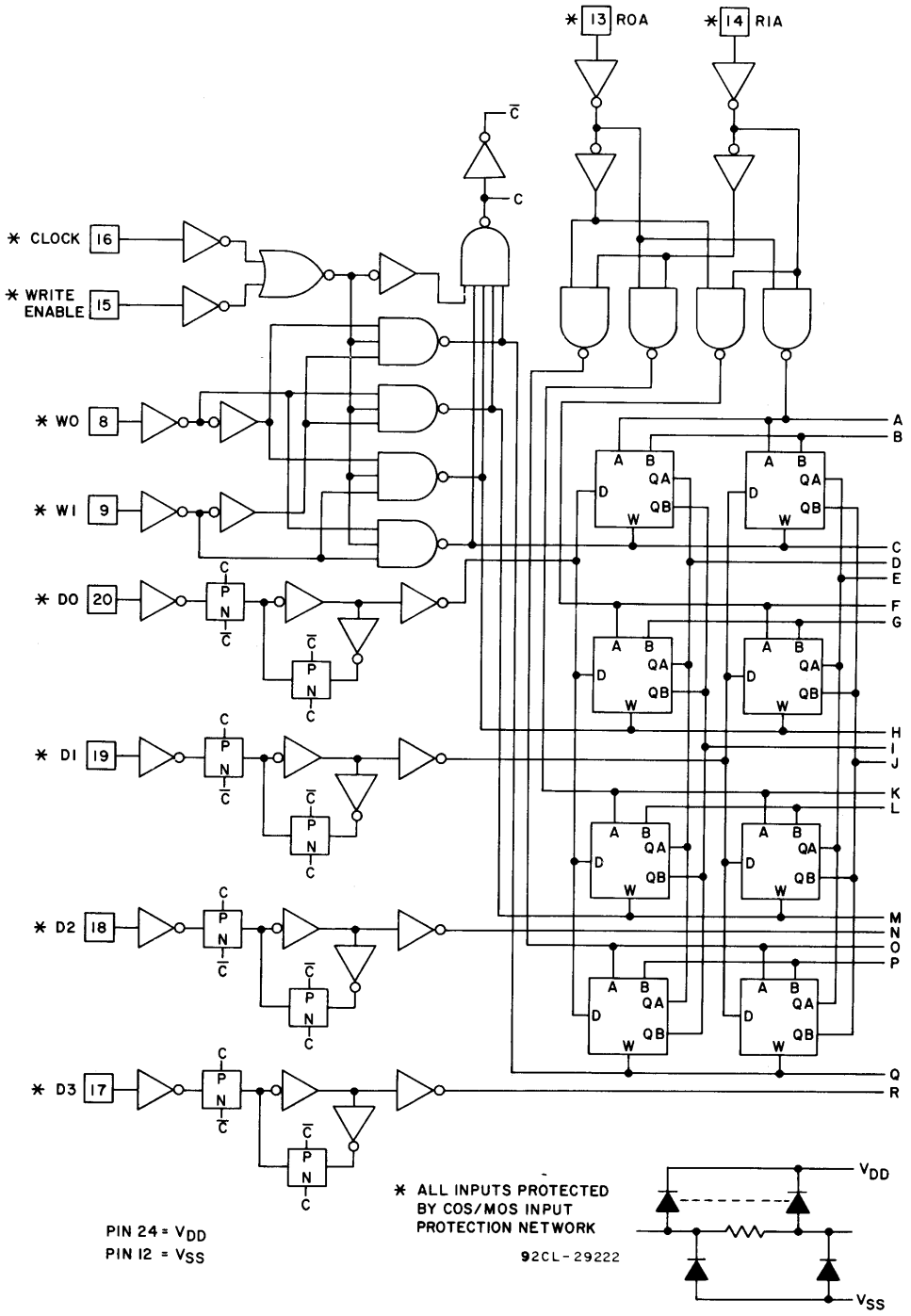


Fig. 148(a) – Logic diagram for the CD40208 4x4 multiport register (continued on next page).

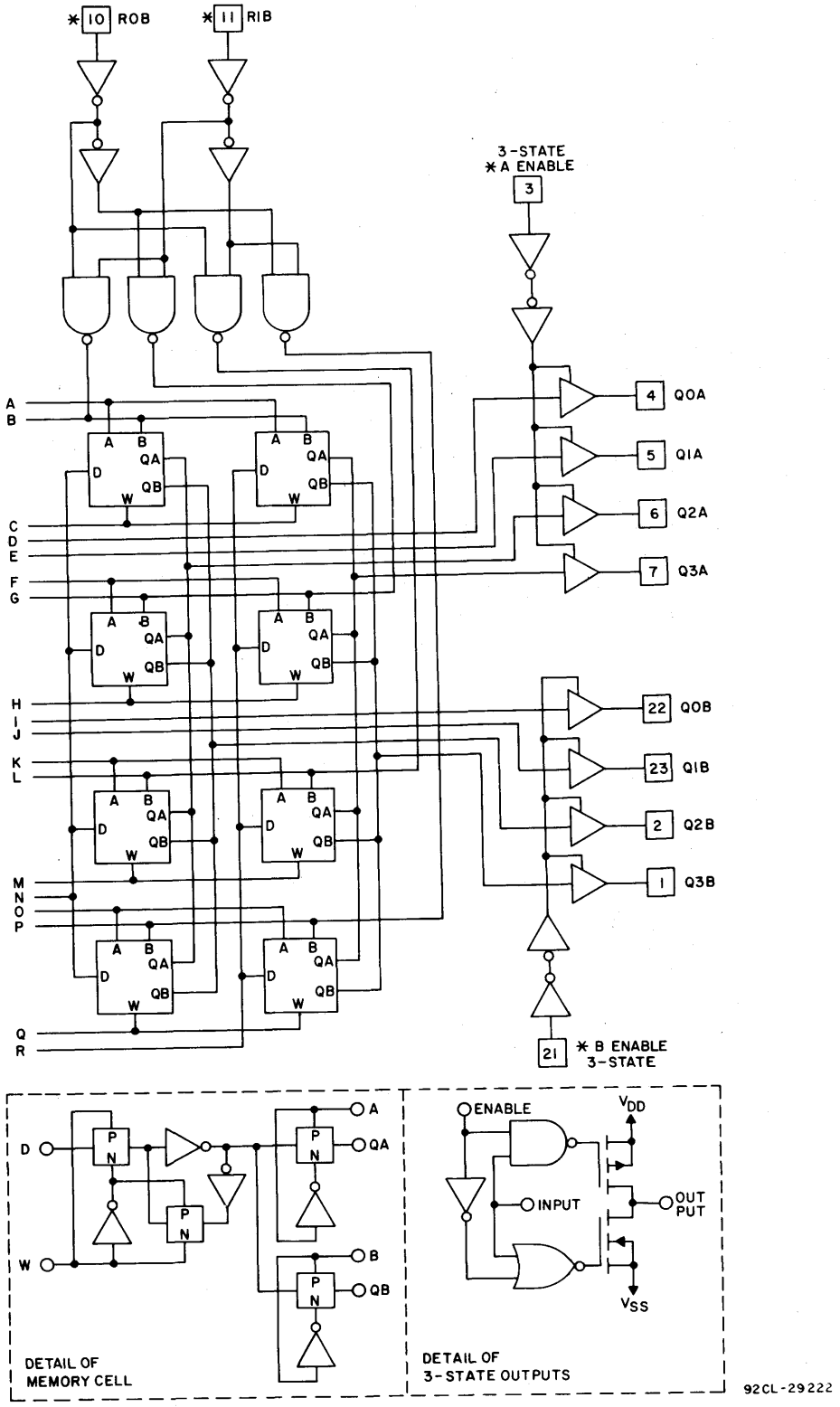


Fig. 148(a) — Logic diagram for the CD40208 4x4 multiport register (continued from preceding page).

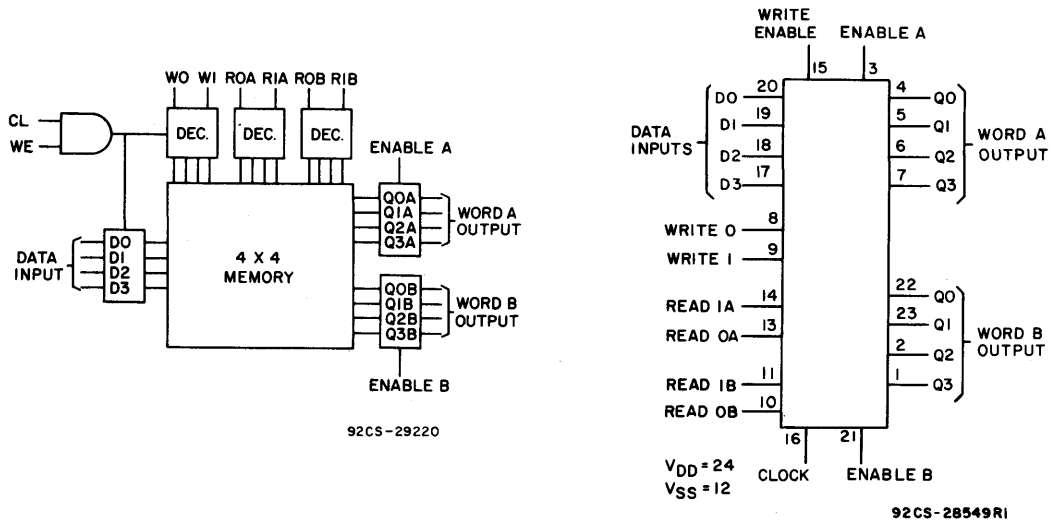


Fig. 148(b) – Block and functional diagrams for the CD40208 4x4 multiport register.

makes it possible to connect the outputs to the bus lines in a bus-organized system without the need for interface or pull-up components.

The truth table for the CD40208 is shown in Fig. 149. When the write-enable input is high, all data input lines are latched on the positive transition of the clock and the data is entered into the word selected by the write address lines. When write-enable is low, the clock is inhibited and no new data is entered. In either case, the contents of any word may be accessed by means of the read address lines independent of the state of the clock input.

FIFO BUFFER REGISTER

Fig. 150 shows the functional and block diagrams of the CD40105 low-power 4-bit-wide-by-16-bit-long first-in-first-out (FIFO) register. The 4 x 16 data register in this device is under constant control of a large network. Each word position in the array is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled, and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	D_n	Q_{nA}	Q_{nB}
⌐	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⌐	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
⌐	1	0	0	0	1	1	0	1	1	D_n to word 0	Word 1 out	Word 2 out
⌐	0	0	0	0	1	1	0	1	1	Word 0 not altered	Word 1 out	Word 2 out
X	X	X	X	1	0	0	1	1	1	X	Word 2 out	Word 1 out
⌐	X	X	X	X	X	X	X	1	1	X	NC	NC

1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE, Z = HIGH IMPEDANCE
S1 and S2 refer to input states of either 1 or 0

Fig. 149 – Truth table for the CD40208 multiport register.

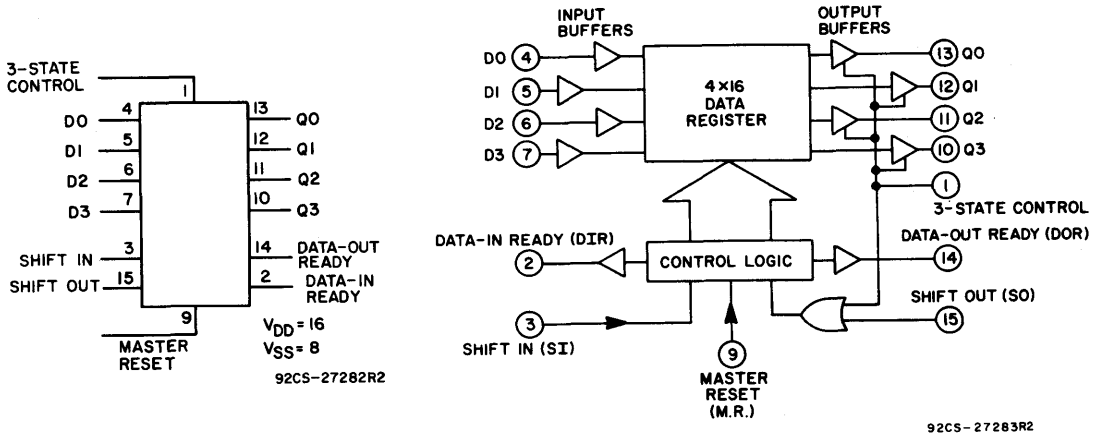


Fig. 150 – Functional and block diagrams for the CD40105 FIFO register.

flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse, transferring data from the preceding four data latches into its own four data latches and resetting the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs.

Because all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (data-in ready) indicates whether the FIFO register is full, and the status of the last flip-flop (data-out ready) indicates whether the register contains data. Because the earliest data are removed from the bottom of the data stack (the output end), all data entered later automatically propagate (ripple) toward the output.

BINARY RIPPLE-CARRY COUNTERS

7-Stage Binary Counter with Buffered Reset

The CD4024, shown in Fig. 151, consists of an input-pulse-shaping circuit, reset line driver circuitry, and seven binary counter stages. The counter is reset to zero by a high level on the reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse. All inputs and outputs are buffered.

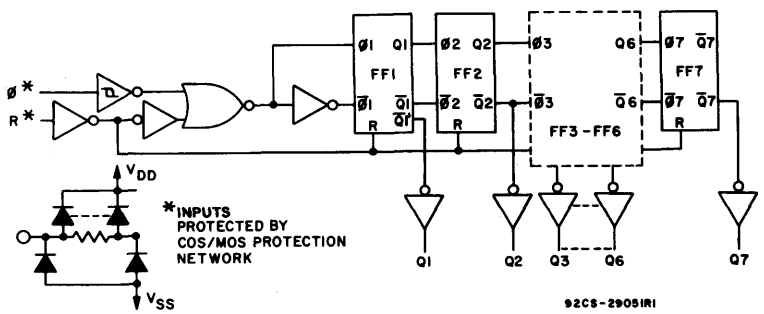


Fig. 151(a) – Logic diagram for the CD4024 7-stage binary counter.

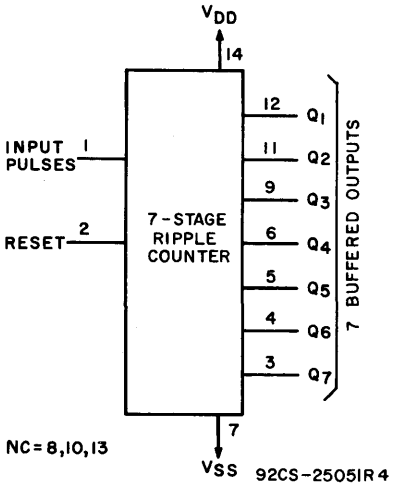


Fig. 151(b) — Functional diagram for the CD4024 7-stage binary counter.

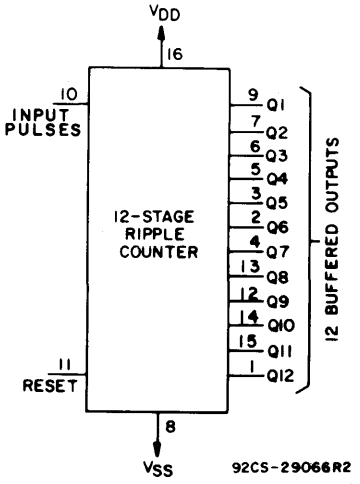


Fig. 152(b) — Functional diagram for the CD4040 12-stage binary counter.

12-Stage Ripple-Carry Binary Counter/Divider

The CD4040 consists of an input-pulse-shaping circuit, reset line driver circuitry, and 12 ripple-carry binary counter stages, as shown in Fig. 152. Resetting the counter to the all-zeros state is accomplished by a high level on the reset line. A master-slave flip-flop configuration is used for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are buffered.

14-Stage Ripple-Carry Binary Counter/Divider with Buffered Reset

The CD4020, shown in Fig. 153, consists of an input-pulse-shaping circuit, reset line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are available from stages 1 and 4 through 14. The counter is reset to its all-zeros state by a high level on the reset inverter input line. Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each input pulse.

14-Stage Ripple-Carry Binary Counter/Divider with Oscillator Section

Fig. 154 shows the functional and logic diagrams of the CD4060, which consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A reset input is provided which resets the counter to the all-zeros state and disables the oscillator. A high

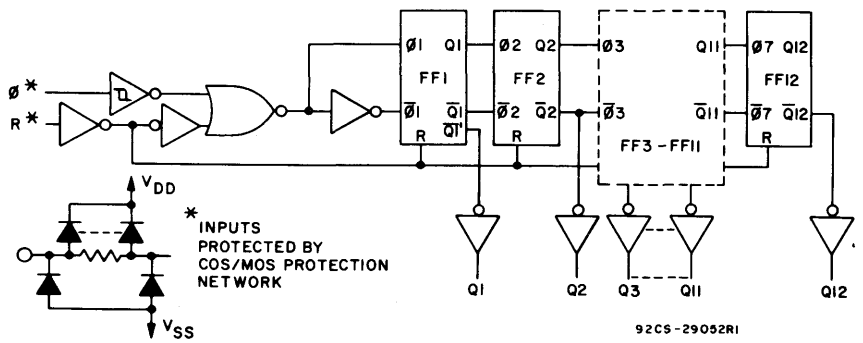


Fig. 152(a) — Logic diagram for the CD4040 12-stage binary counter.

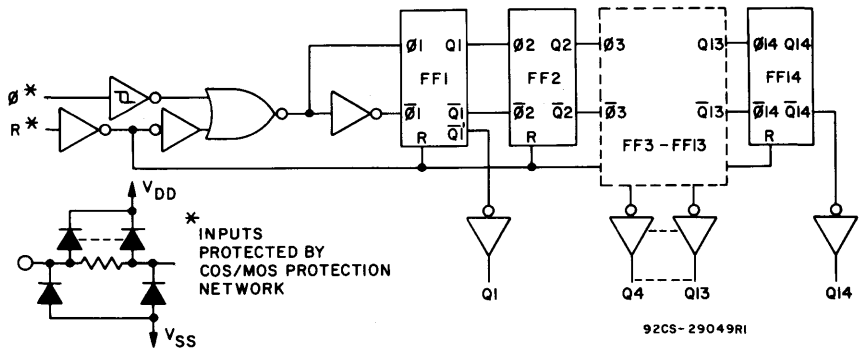


Fig. 153(a) – Logic diagram for the CD4020 14-stage binary counter.

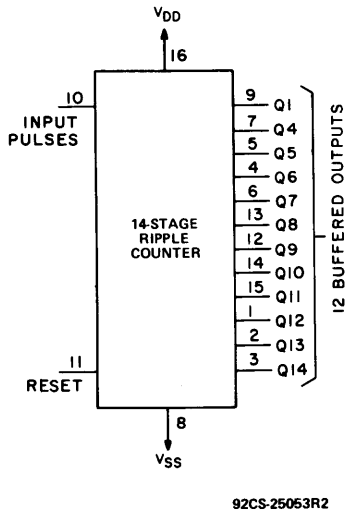


Fig. 153(b) – Functional diagram for the CD4020 14-stage binary counter.

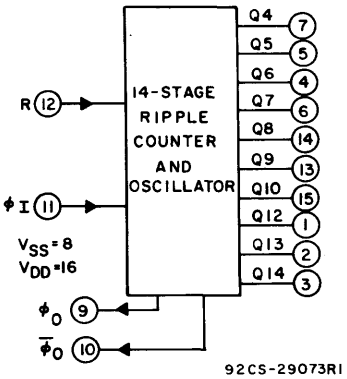


Fig. 154(a) – Functional diagram for the CD4060 14-stage binary counter with oscillator.

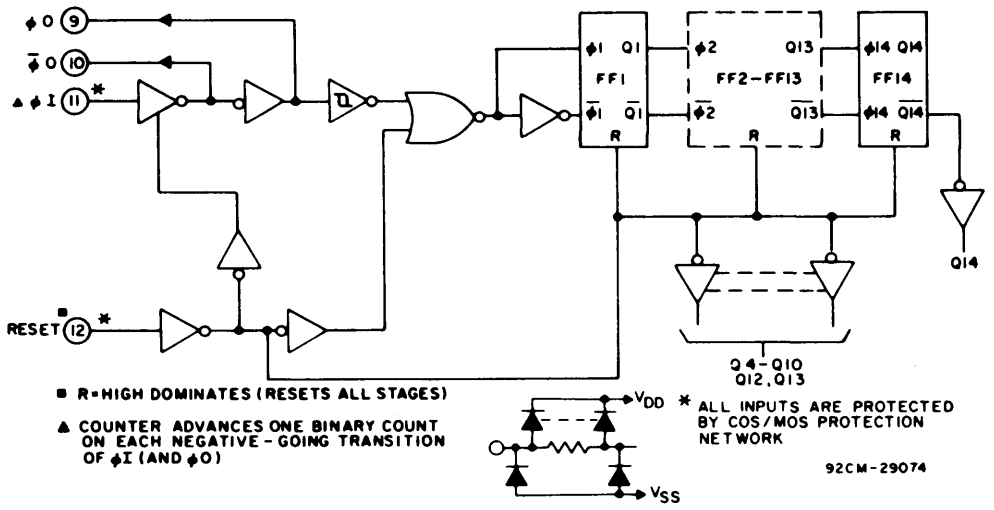


Fig. 154(b) – Logic diagram for the CD4060 14-stage binary counter with oscillator.

level on the reset line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative-going transition of the clock signal. All inputs and outputs are buffered.

CLOCK TIMER

The CD4045 is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, three 5.5-V zener diodes (which provide transient protection at 16.5 V), and input inverters for use in a crystal oscillator. The CD4045 configuration, shown in Fig. 155, provides 21 flip-flop counting stages and two flip-flops for shaping the output waveform for a 3.125-percent duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p-channel and n-channel transistors are brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_P to V_{DD}, S_N to V_{SS}).

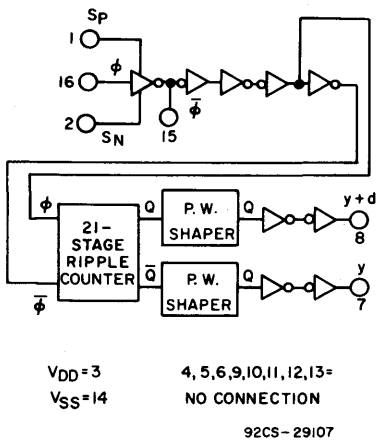


Fig. 155(a) — Functional diagram for the CD4045 timing circuit.

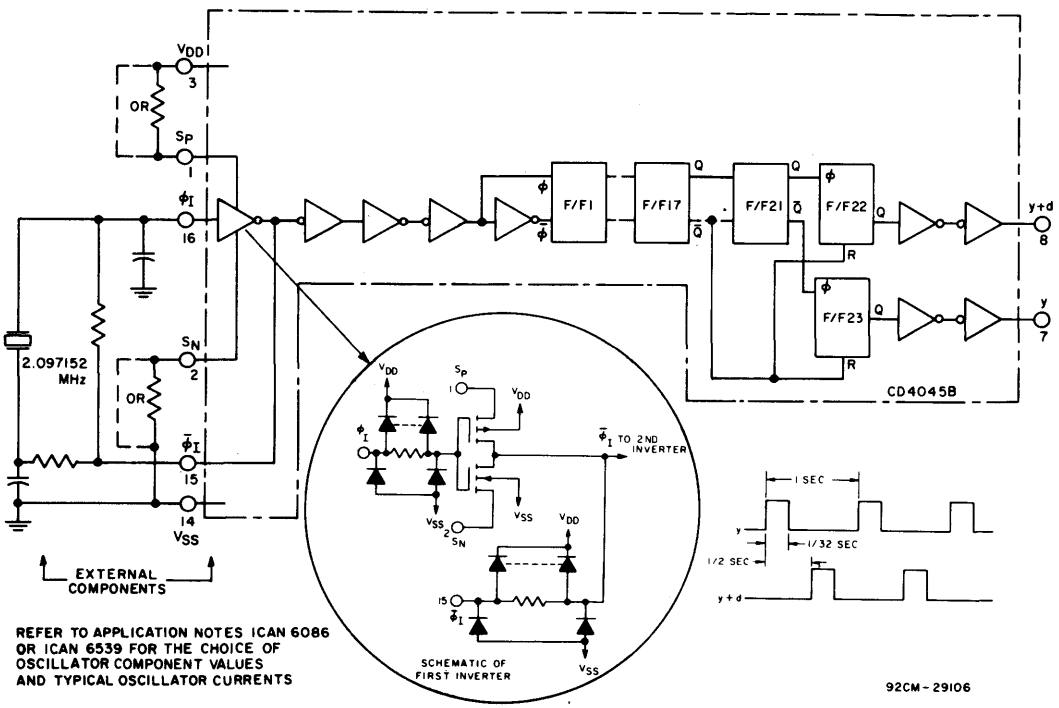


Fig. 155(b) — Logic diagram for the CD4045 timing circuit.

SYNCHRONOUS COUNTERS

5-Stage Decade Counter/Divider with 10 Decoded Decimal Outputs

Fig. 156 shows the functional and logic diagrams of the CD4017, which consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a clock, a reset, and a clock-inhibit signal.

The decade counter is advanced one count at the positive-going clock-signal transition if the clock-inhibit signal is low. Counter advancement by means of the clock line is inhibited when the clock-inhibit signal is high. A high reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high-speed operation, 2-input decimal decode

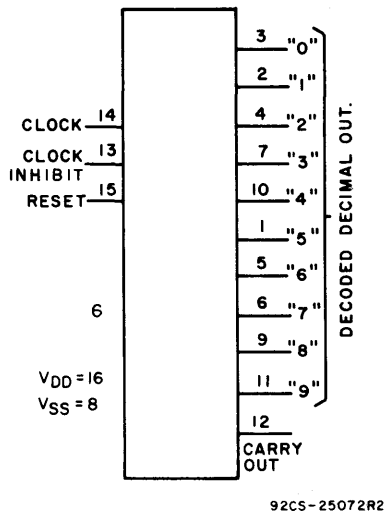


Fig. 156(a) — Functional diagram for the CD4017 5-stage decade counter/divider.

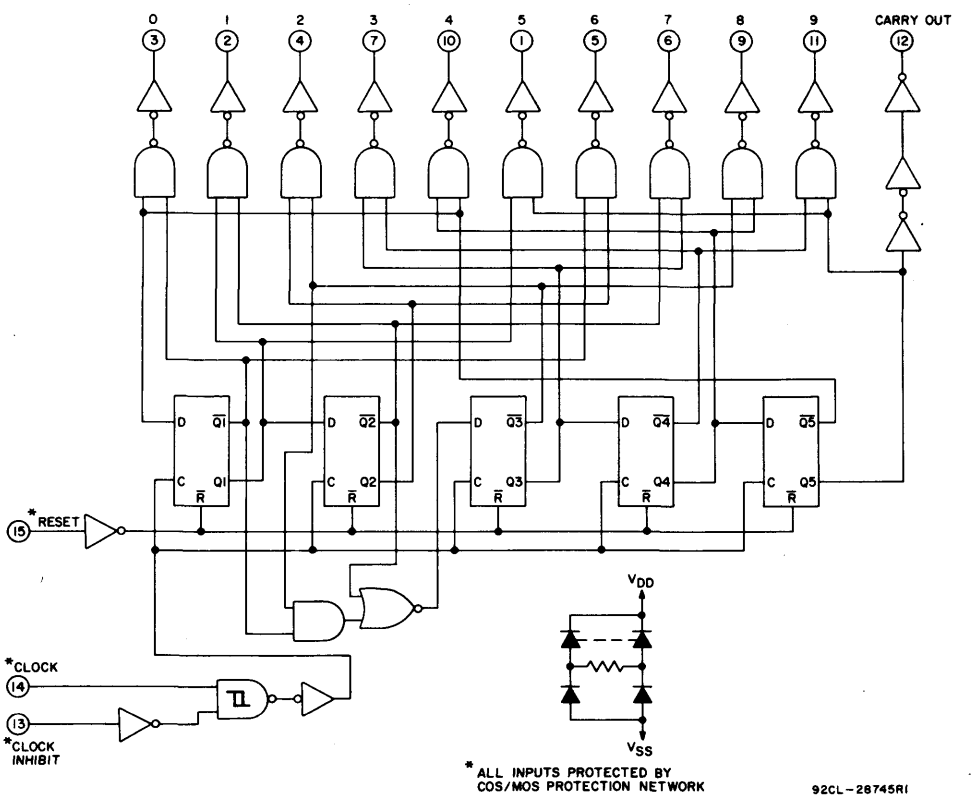


Fig. 156(b) — Logic diagram for the CD4017 5-stage decade counter/divider.

gating, and spike-free decoded outputs. Anti-lock gating is provided to assure proper counting sequence. The ten decoded outputs are normally low and go high only at their respective decimal time slots. Each decoded output remains high for one full clock cycle. A carry-out signal completes one cycle for every 10 clock-input cycles, and is used to clock the succeeding device directly in a multi-device counting chain.

4-Stage Divide-by-8 Counter/Divider with 8 Decoded Outputs

The CD4022 consists of a 4-stage divide-by-8 Johnson counter, associated decode output gating, and a carry-out bit, as shown in Fig. 157. The counter is cleared to its zero count

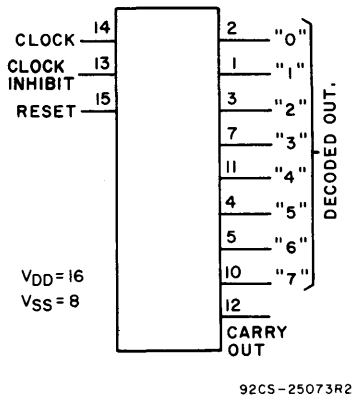


Fig. 157(a) – Functional diagram for the CD4022 4-stage divide-by-eight counter/divider.

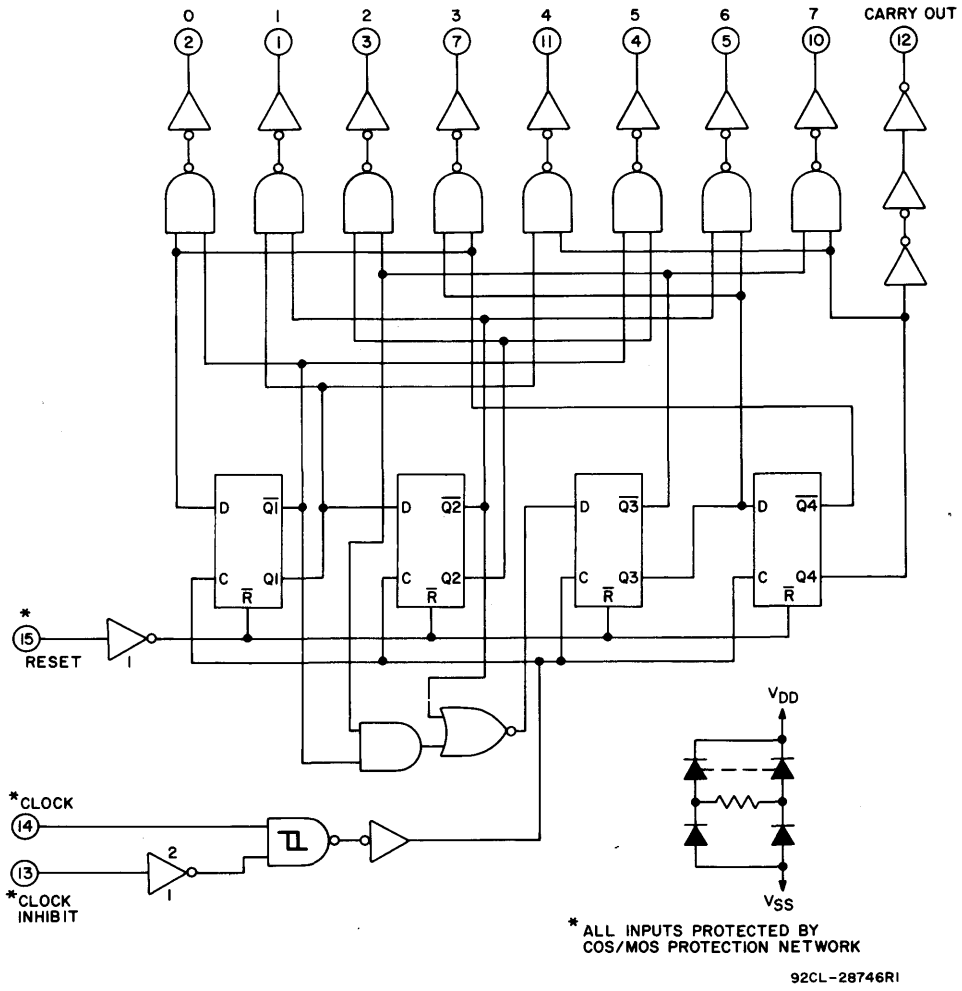


Fig. 157(b) – Logic diagram for the CD4022 4-stage divide-by-eight counter/divider.

by a high reset signal. The counter is advanced at the positive-going clock-signal transition if the clock-inhibit signal is low.

Use of the Johnson divide-by-8 counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoder outputs. Anti-lock gating is provided to assure proper counting sequence. The 8 decode gating outputs are normally low and go high only at their respective decoded time slots. Each decoded output remains high for one full clock cycle. The carry-out signal completes one cycle for 8 clock-input cycles, and is used as a ripple-carry signal to directly clock a succeeding counter device in a multi-device counting system.

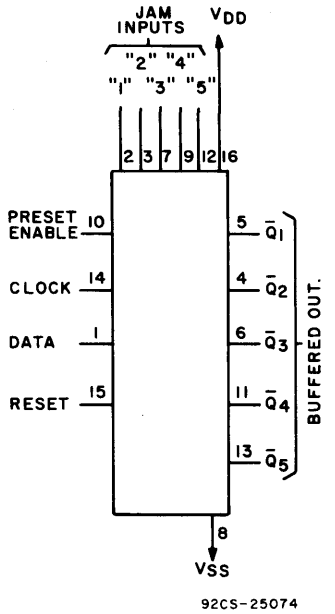


Fig. 158(a) — Functional diagram for the CD4018 5-stage presettable divide-by-N counter.

5-Stage Presettable Divide-by-N Counter

Fig. 158 shows the functional and logic diagrams of the CD4018. This type consists of 5 Johnson counter stages, buffered Q

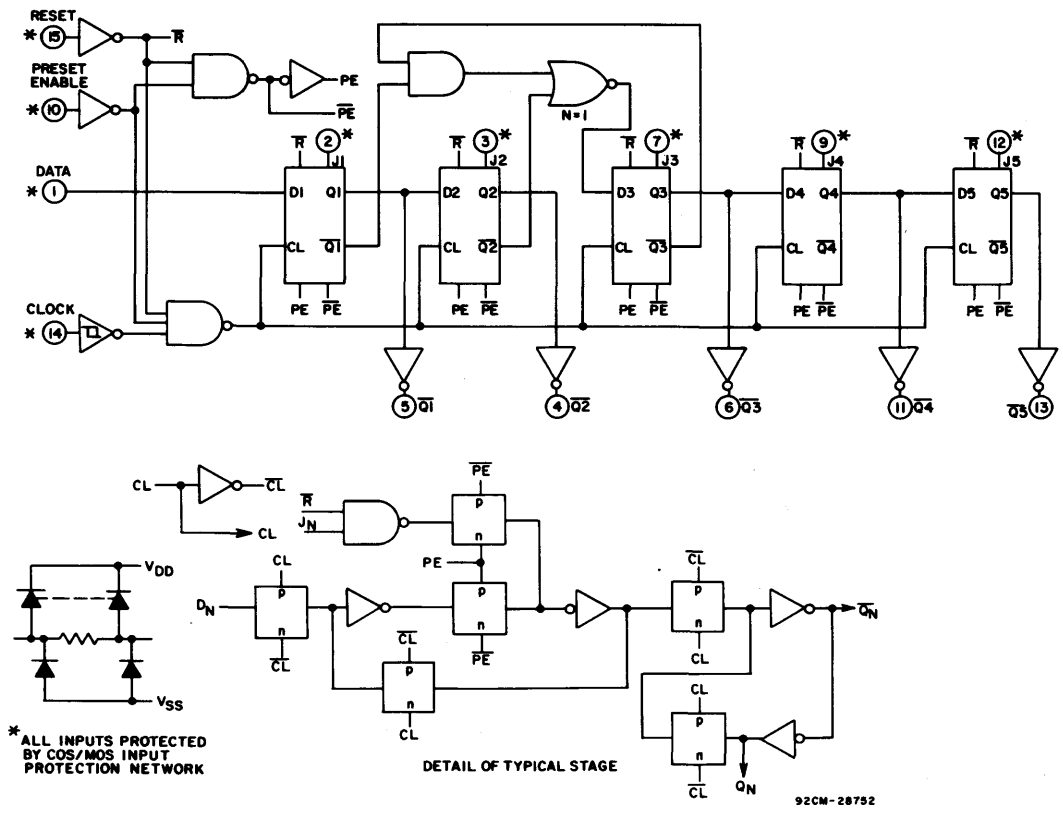


Fig. 158(b) — Logic diagram for the CD4018 5-stage presettable divide-by-N counter.

outputs from each stage, and counter preset control gating. Clock, reset, data, preset enable, and 5 individual jam inputs are provided. Divide-by-10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the Q5, Q4, Q3, Q2, or Q1 signals, respectively, back to the data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011 gate package to properly gate the feedback connection to the data input.

Divide-by functions greater than 10 can be achieved by use of multiple CD4018 units. The counter is advanced one count at the positive clock-signal transition. A high reset signal clears the counter to an all-zero condition. A high preset-enable signal allows information on the jam inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

4-Stage Binary or BCD Presettable Up/Down Counter

The CD4029 consists of a four-stage binary or BCD-decade up/down counter, as shown in Fig. 159, with provisions for look-ahead carry in both counting modes. The inputs consist of a single clock, carry-in (clock inhibit), binary/decade, up/down, and preset enable; four individual jam signals and a carry-out signal are provided as outputs.

A high preset-enable signal allows information on the jam inputs to preset the counter to any state asynchronously with the clock. A low on each jam line when the preset-enable signal is high resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the carry-in and preset-enable signals are low. Advancement is inhibited

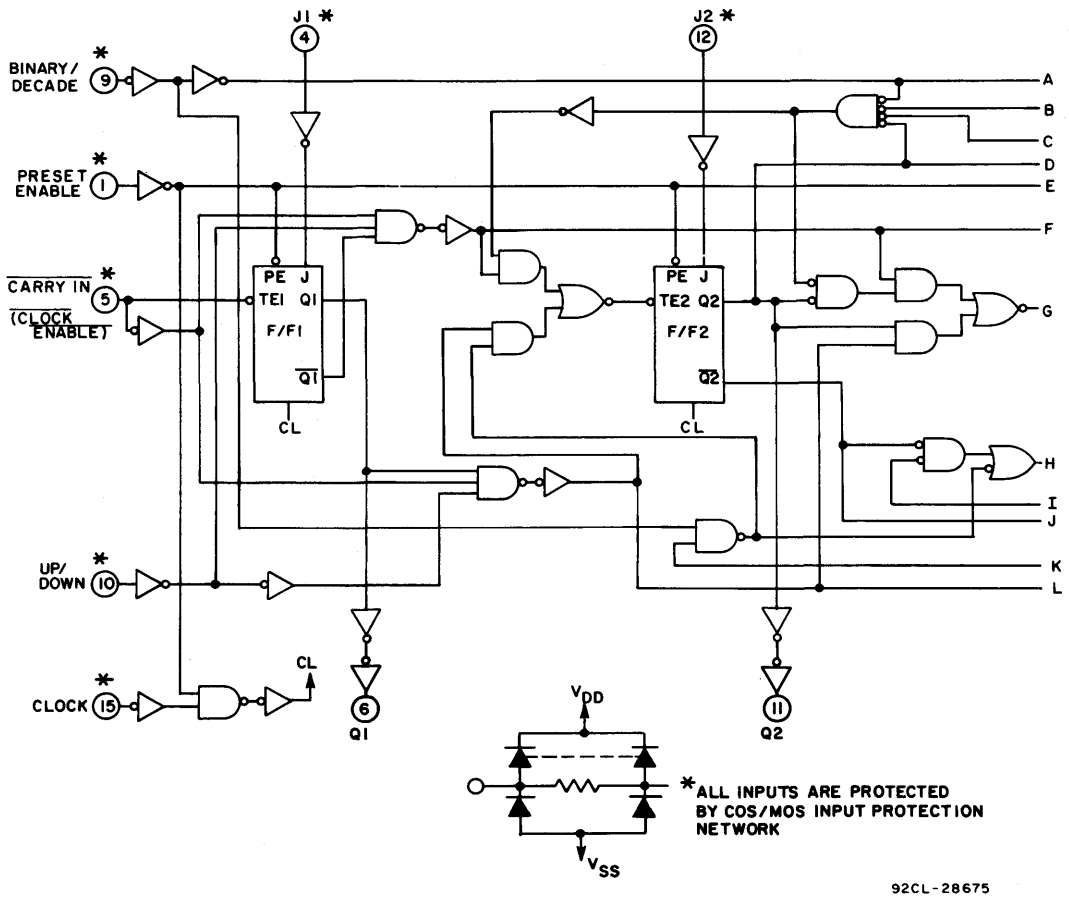


Fig. 159(a) – Logic diagram for the CD4029 presettable up/down counter (continued on next page).

when the carry-in or preset-enable signals are high.

The carry-out signal is normally high, and goes low when the counter reaches its maximum count in the up mode or the minimum count in the down mode, provided the carry-in signal is low. The carry-in signal in the low state can thus be considered a clock inhibit. The carry-in terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the binary/decade input is high; the counter counts in the decade mode when the binary/decade input is low. The counter counts up when the up/down input is high and down when the up/down input is low.

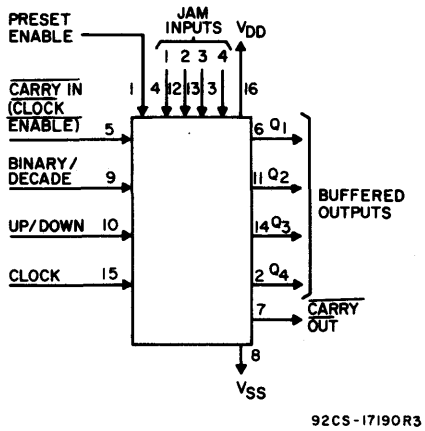
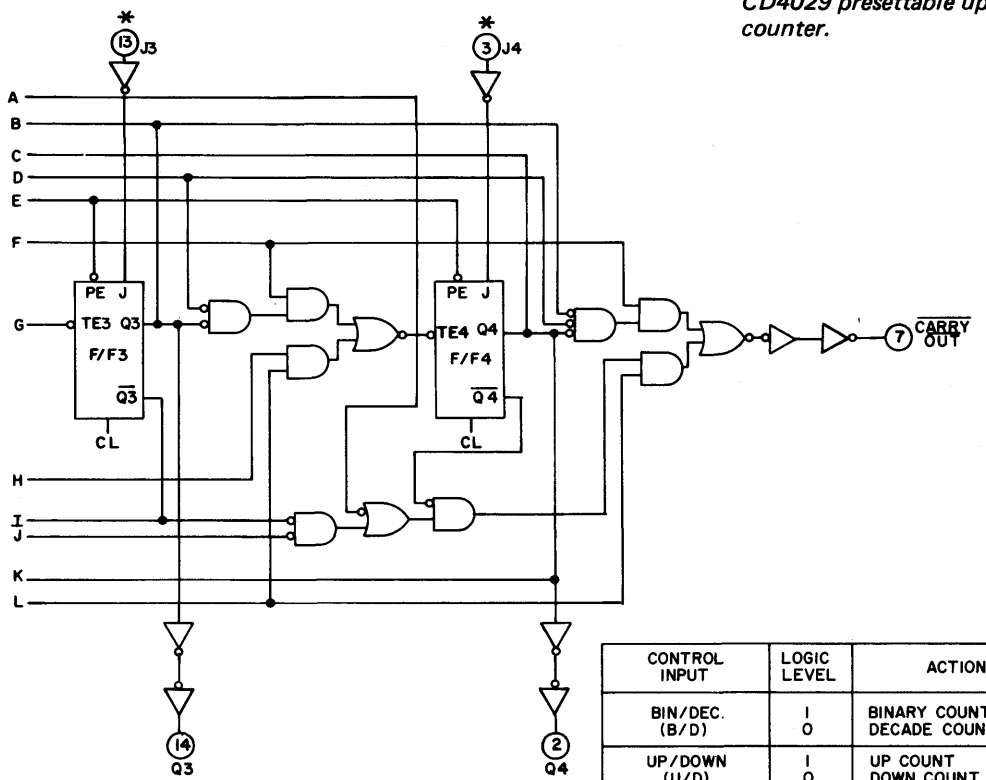
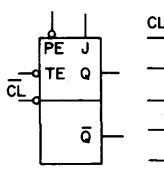


Fig. 159(b) — Functional diagram for the CD4029 presettable up/down counter.



TRUTH TABLE



CLOCK	TE	PE	J	Q	Q̄
X	X	0	0	0	1
↓	0	1	X	Q̄	Q
X	X	0	1	1	0
↓	1	1	X	Q	Q̄ NC
↑	X	1	X	Q	Q̄ NC

X-DON'T CARE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
CARRY IN (CI) (CLOCK ENABLE)	1	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION
	0	ADVANCE COUNTER AT POS. CLOCK TRANSITION

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Fig. 159(a) — Logic diagram for the CD4029 presettable up/down counter (continued from preceding page).

Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangements. Parallel clocking provides synchronous control and thus faster response from all counting outputs. Ripple counting allows for longer clock input rise and fall times.

4-Stage Presettable Up/Down Counters

The CD4510 and CD4516 presettable up/down counters consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters, as shown in Fig. 160. The CD4510 is a BCD counter; the CD4516 is a binary one.

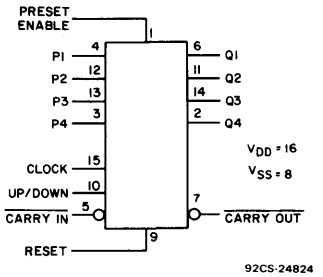


Fig. 160(a) – Functional diagram for the CD4510 and CD4516 presettable up/down counters.

These counters can be cleared by a high level on the reset line, and can be preset to any binary number present on the jam inputs

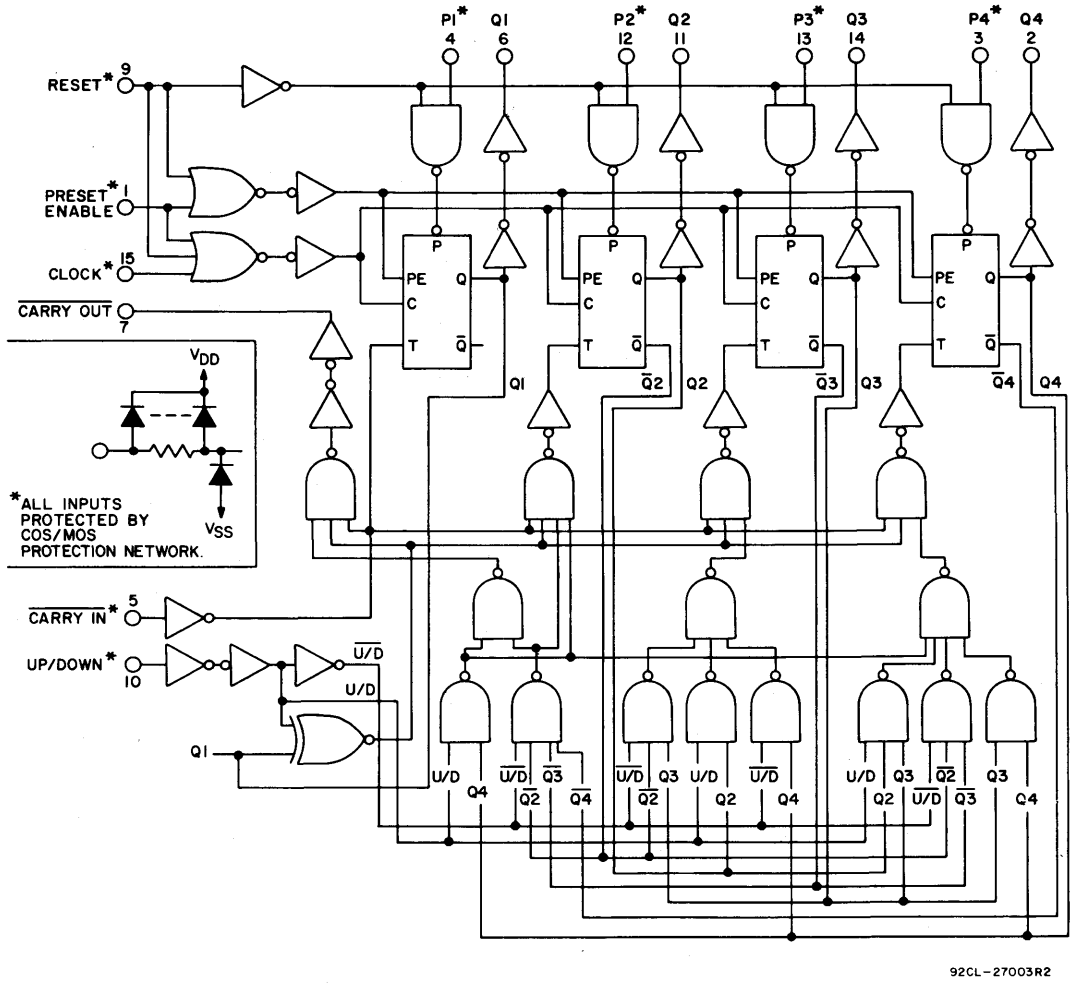


Fig. 160(b) – Logic diagram for the CD4510 presettable up/down BCD counter.

by a high level on the preset-enable line. The CD4510 will count out of non-BCD counter states in a maximum of two clock pulses in the up mode and a maximum of four clock pulses in the down mode.

If the carry-in input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the carry-out of a less significant stage to the carry-in of a more significant stage.

The CD4510 and CD4516 can be cascaded in the ripple mode by connecting the carry-out line to the clock of the next stage. If the up/down input changes during a terminal count, the carry-out must be gated with the clock, and the up/down input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

8-Stage Presettable Synchronous Down Counter

Fig. 161 shows the functional diagram and truth table for the CD40102 and CD40103, which consist of an 8-stage synchronous down-counter with a single output which is active when the internal count is zero. The CD40102 is configured as two cascaded BCD stages, as shown in Fig. 162; the CD40103 contains a single 8-bit binary counter, as

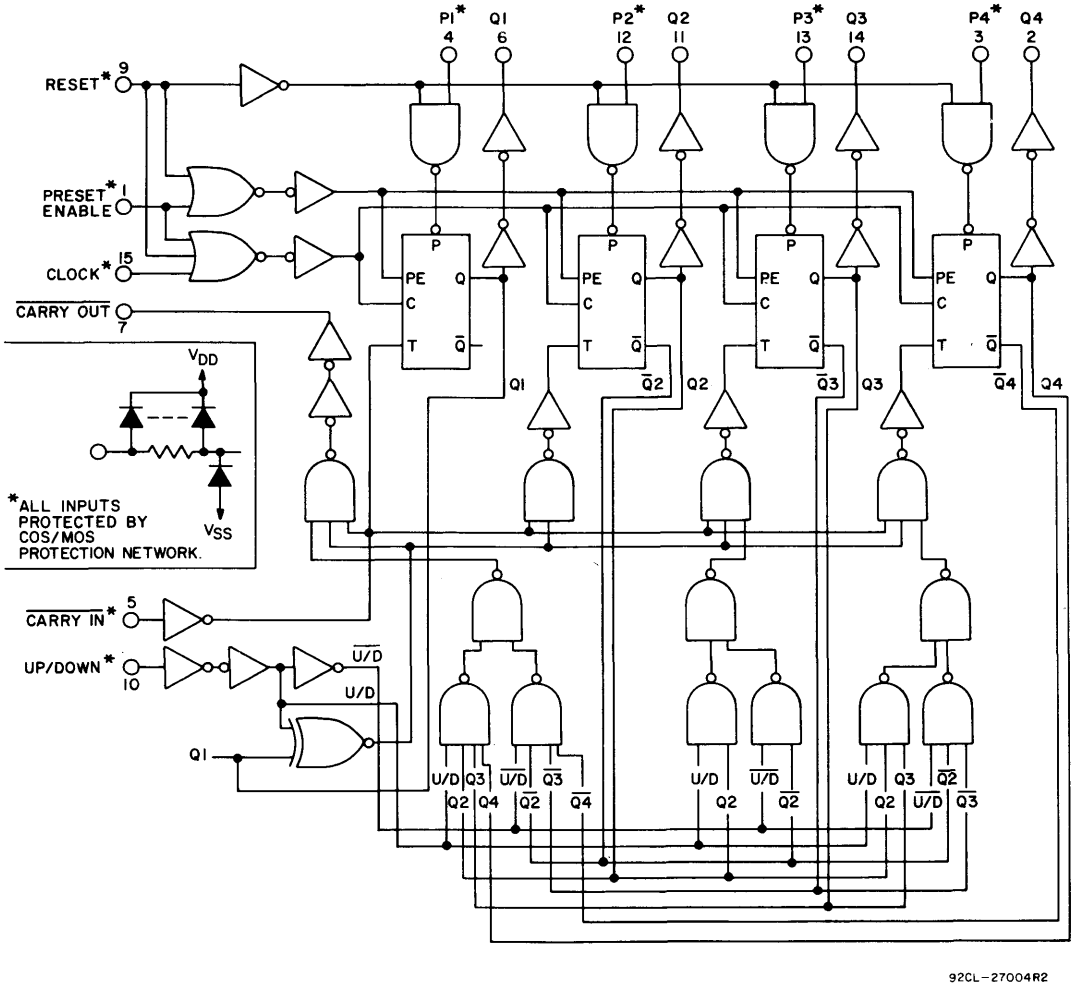


Fig. 160(c) — Logic diagram for the CD4516 presettable up/down binary counter.

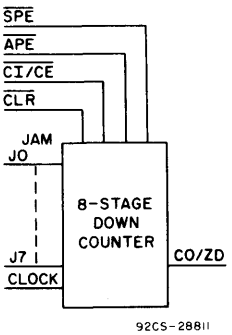


Fig. 161(a) — Functional diagram for the CD40102 and CD40103 presettable synchronous down-counters.

clock transition regardless of the state of the CI/CE input. When the asynchronous preset-enable (APE) input is low, data at the jam inputs are asynchronously forced into the counter regardless of the state of the SPE, CI/CE, or clock inputs. Jam inputs J0-J7 represent two 4-bit BCD words for the CD40102 and a single 8-bit binary word for the CD40103. When the clear (CLR) input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the CD40102 and 255_{10} for the CD40103) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table shown in Fig. 161.

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
1	1	1	1	Synchronous	Inhibit counter
1	1	1	0		Count down
1	1	0	X		Preset on next positive clock transition
1	0	X	X	Asynchronous	Preset asynchronously
0	X	X	X		Clear to maximum count

Notes: 1. 0 = Low level
1 = High level
X = Don't care
2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. JAM inputs: CD40102B BCD; MSD = J7,J6,J5,J4 (J7 is MSB)
LSD = J3,J2,J1,J0 (J3 is MSB)
CD40103B Binary; MSB = J7, LSB = J0

Fig. 161(b) — Truth table for the CD40102 and CD40103 presettable synchronous down-counters.

shown in Fig. 163. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the carry-out/zero-detect output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the clock. Counting is inhibited when the carry-in/clock-enable (CI/CE) input is high. If the CI/CE input is low, the carry-out/zero-detect (CO/ZD) output goes low when the count reaches zero and remains low for one full clock period.

When the synchronous preset-enable (SPE) input is low, data at the jam input is clocked into the counter on the next positive

The CD40102 and CD40103 may be cascaded, using the CI/CE input and the CO/ZD output, in either a synchronous or ripple mode.

4-Stage Presettable Up/Down Counter

The CD40192 and CD40193 presettable up/down counters each consist of four synchronously clocked, gated D-type flip-flops connected as counters, as shown in Fig. 164. The inputs consist of four individual jam lines, a preset-enable control, individual clock-up and clock-down inputs, and a master reset. Four buffered Q signal outputs are provided, as well as carry and borrow outputs for multiple-stage counting.

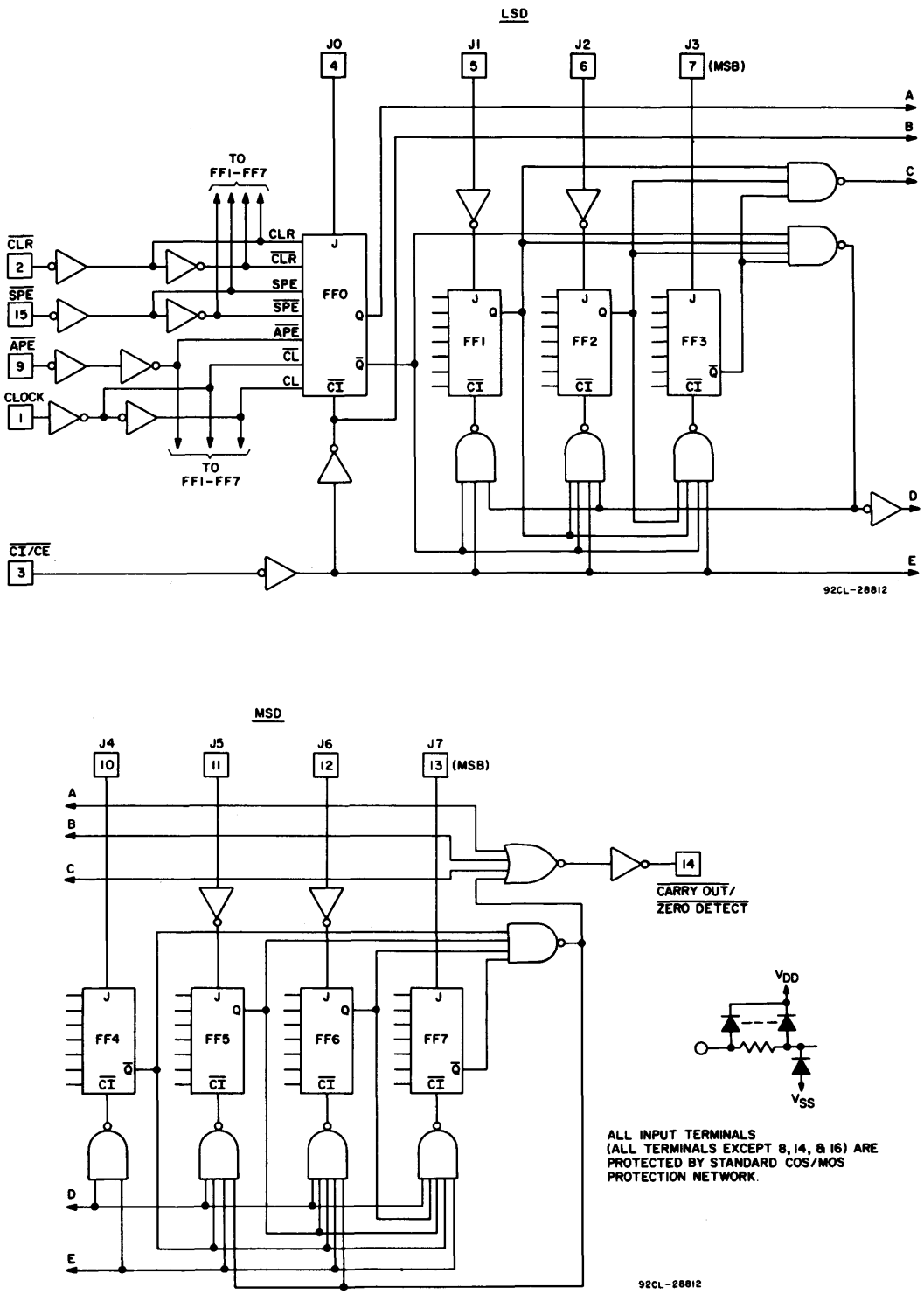


Fig. 162 – Logic diagram for CD40102 BCD down-counter.

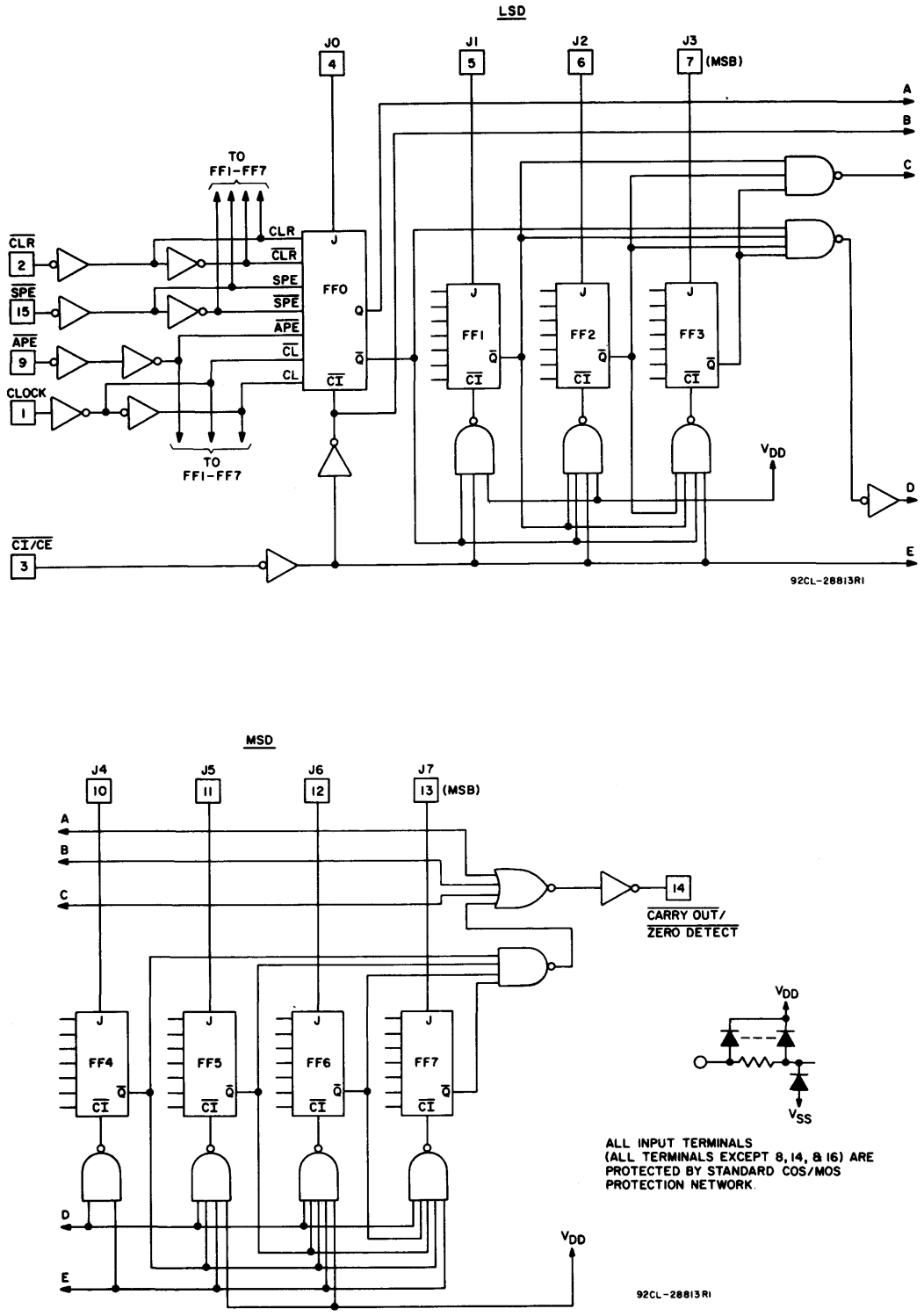


Fig. 163 – Logic diagram for CD40103 binary down-counter.

The counter can be cleared so that all outputs are in a low state by a high on the reset line. A reset can be accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the preset-enable control is low.

The counter counts up one count on the positive clock edge of the clock-up signal, provided the clock-down line is high. The counter counts down one count on the positive clock edge of the clock-down signal, provided the clock-up line is high.

Both the carry and borrow signals are normally high. The carry signal goes low when the counter reaches its maximum count in the count-up mode. The borrow signal goes low when the counter reaches its minimum count in the count-down mode.

Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the borrow and carry outputs to the clock-down and clock-up inputs, respectively, of the succeeding counter package.

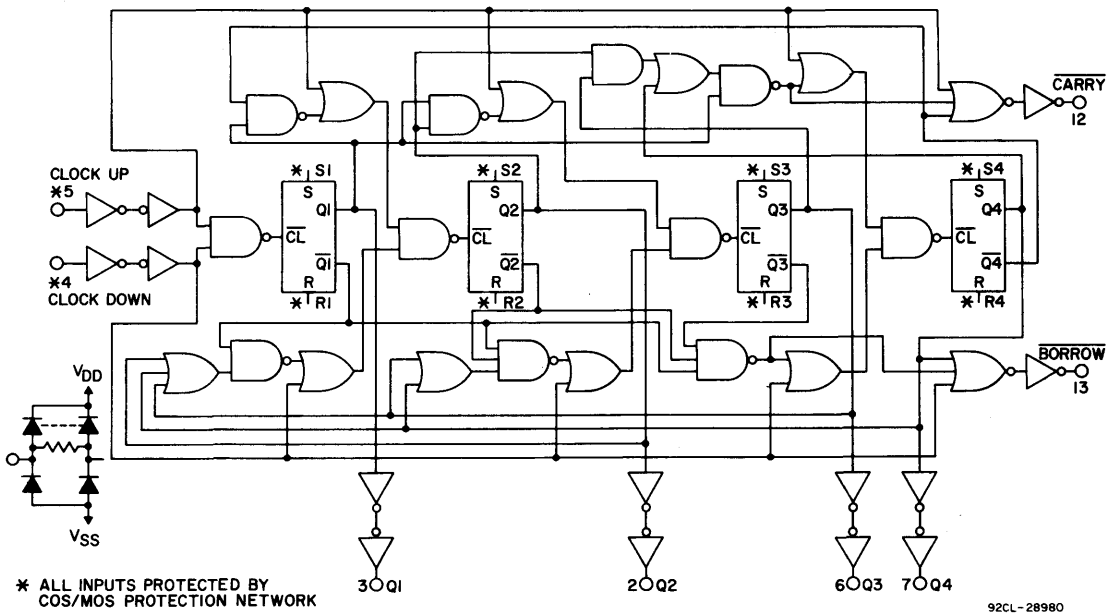


Fig. 164(a) – Logic diagram for the CD40192 presettable up/down BCD counter.

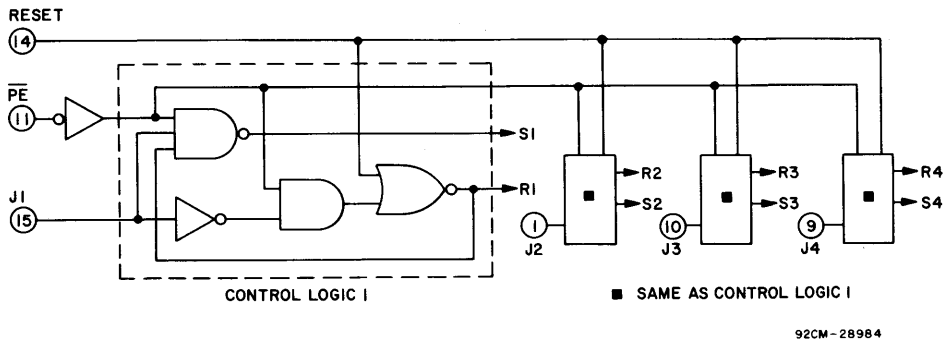


Fig. 164(b) – Control logic detail for the CD40192 and CD40193 presettable up/down counters.

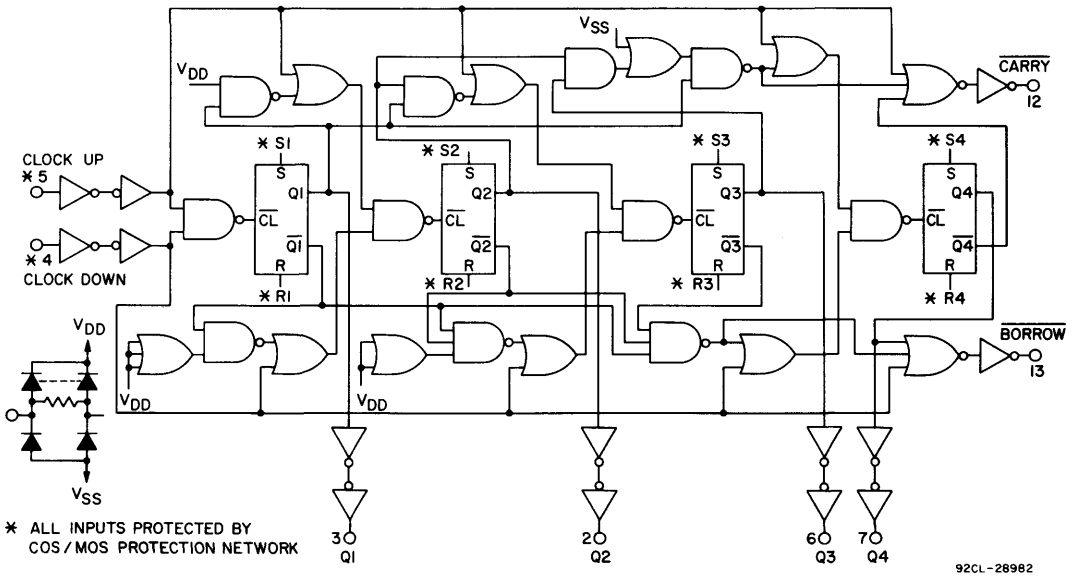


Fig. 164(c) – Logic diagram for the CD40193 presettable up/down binary counter.

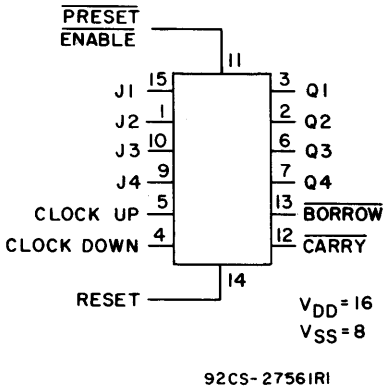


Fig. 164(d) – Functional diagram for the CD40192 and CD40193 presettable up/down counters.

Dual 4-Stage Up-Counters

The CD4518 and CD4520 dual up-counters each consist of two identical internally synchronous 4-stage counters, as shown in Fig. 165; the CD4518 contains BCD counters, and the CD4520 contains binary counters. The counter stages are D-type flip-flops having interchangeable clock and enable lines for incrementing on either the positive-going or negative-going transitions. For single-unit operation, the enable input is maintained high and the counter advances on each positive-going transition of the clock. The counters are cleared by high levels on their reset lines.

These counters can be cascaded in the ripple mode by connecting Q4 to the enable input of a subsequent counter while its clock input is held low.

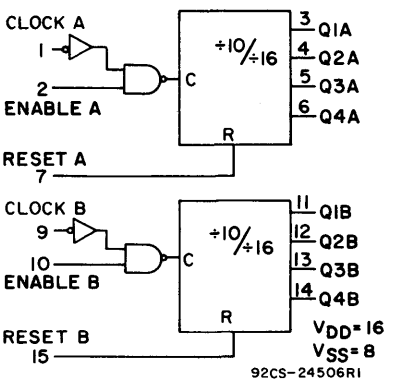


Fig. 165(a) – Functional diagram for the CD4518 and CD4520 4-stage dual up-counters.

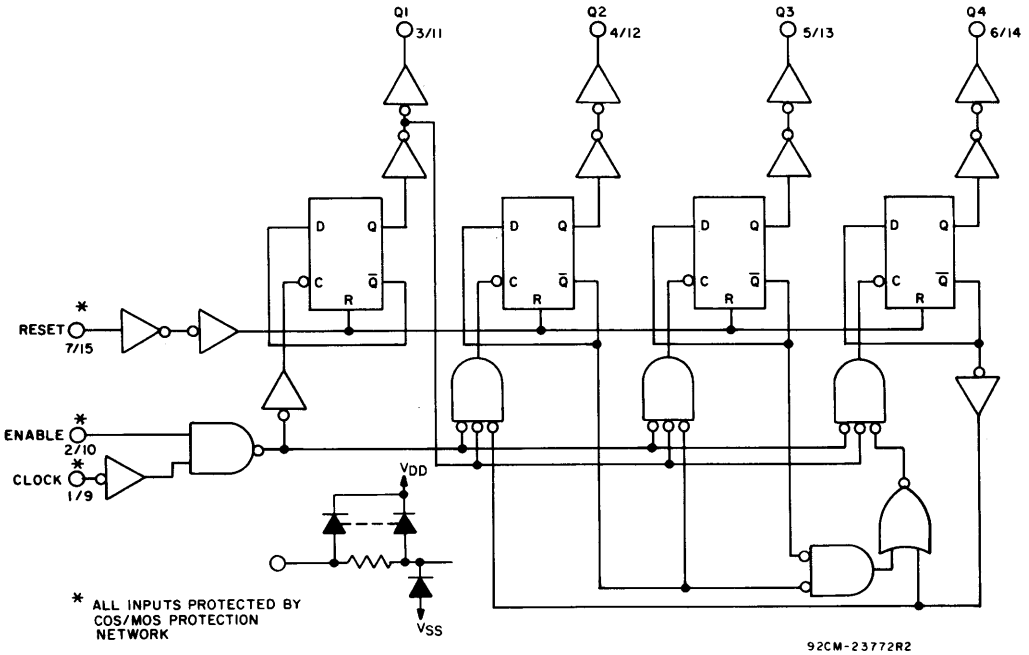


Fig. 165(b) – Logic diagram for one section of the CD4518 BCD dual up-counter.

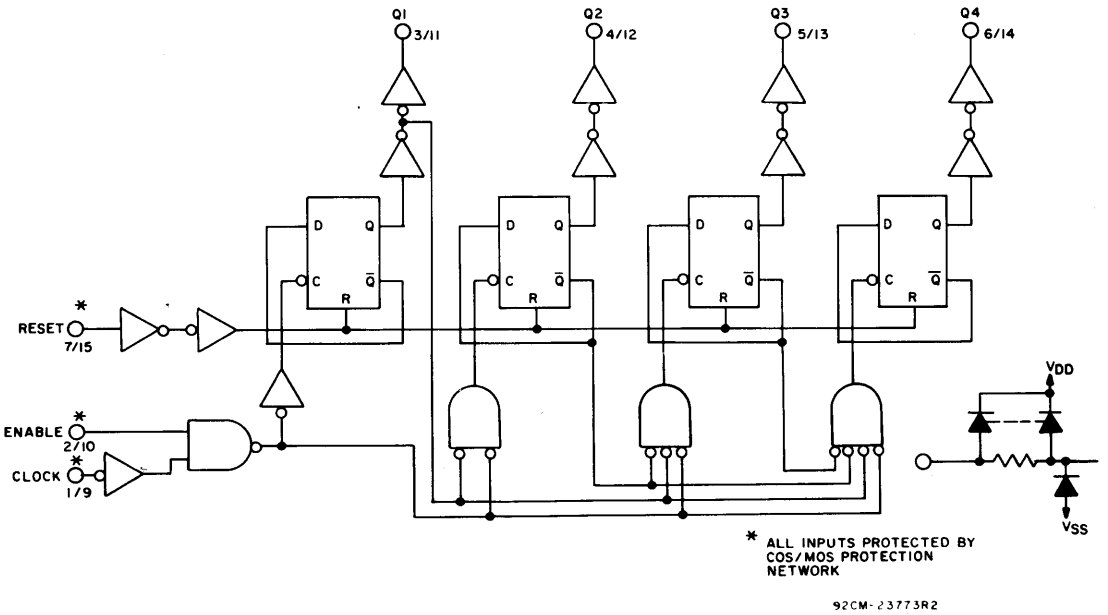


Fig. 165(c) – Logic diagram for one section of the CD4520 binary dual up-counter.

Synchronous Programmable 4-Bit Counters

Fig. 166 shows the functional and logic diagrams for the CD40160, CD40161, CD40162, and CD40163 4-bit synchronous programmable counters. The clear function of the CD40162 and CD40163 is synchronous, and a low level at the clear input sets all four outputs low on the next positive clock edge. The clear function of the CD40160 and CD40161 is asynchronous, and a low level at the clear input sets all four outputs low regardless of the state of the clock, load, or enable inputs. A low level at the load input disables the counter and causes the output to agree with the setup data after the next clock pulse regardless of the enable inputs.

Counting is enabled when both the PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This pulse can be used to enable successive cascaded stages.

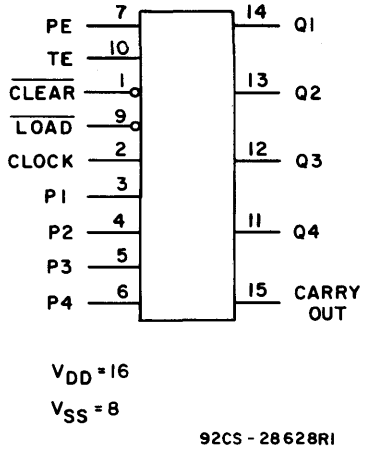


Fig. 166(a) — Functional diagram for the CD40160, CD40161, CD40162, and CD40163 synchronous programmable 4-bit counters.

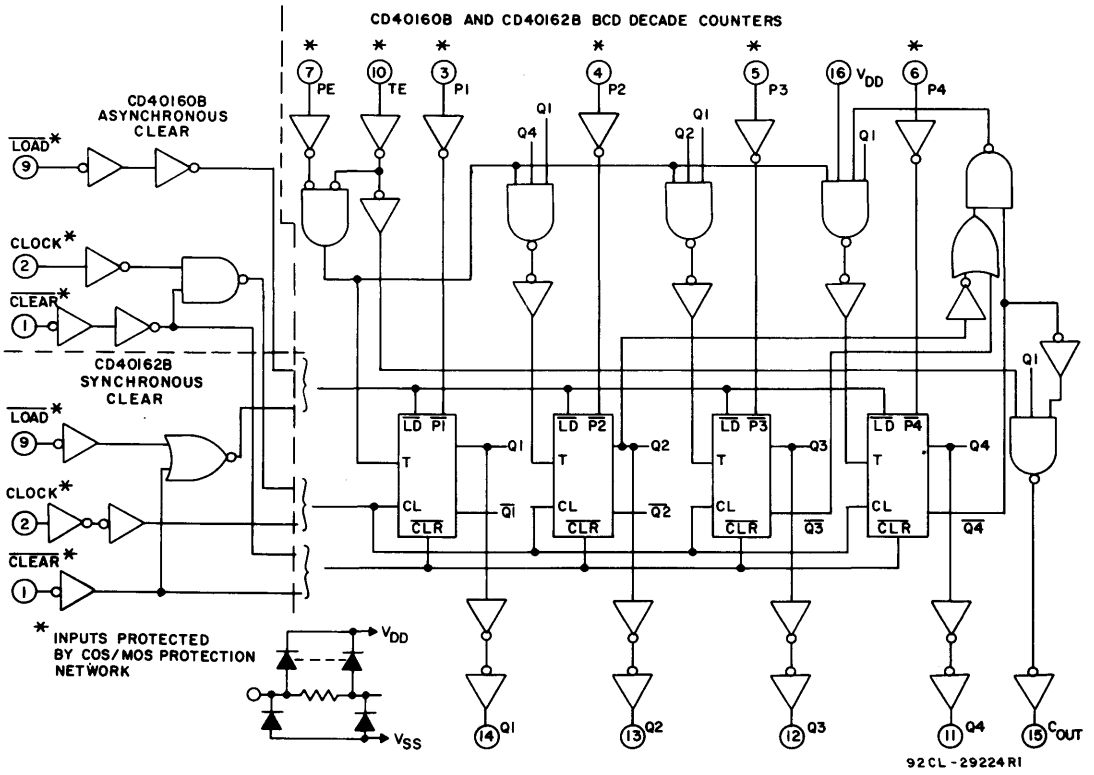


Fig. 166(b) — Logic diagram for the CD40160 and CD40162 programmable BCD decade counters.

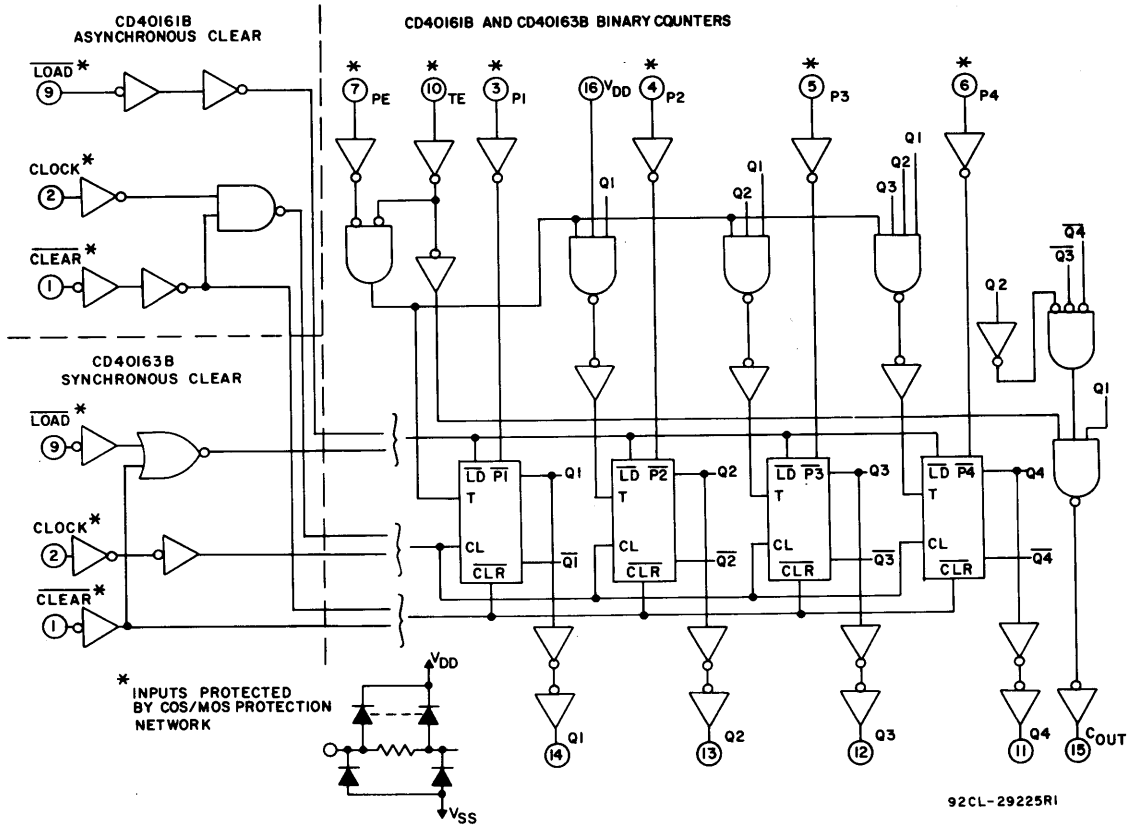


Fig. 166(c) — Logic diagram for the CD40161 and CD40163 programmable binary counters.

IX. Display Drivers

LIQUID-CRYSTAL DISPLAYS

Of all segmented digital displays presently available, liquid-crystal displays (LCD's) are most compatible with COS/MOS circuitry in terms of ultra-low power consumption and operating-voltage ranges. A one-half-inch, 7-segment, 3-1/2 digit liquid-crystal display draws only a few microamperes when all segments are energized.

The first LCD's were dynamic-scattering types which had operating voltages in the range of 12 to 18 volts. The later development of field-effect LCD's reduced operating voltages to the 3-to-7-volt range, further reduced current levels, and improved viewability.

LCD's turn on when a field is applied between a segment and the back electrode, across the liquid-crystal fluid. To avoid plating effects, the field must be periodically reversed (usually at 32 Hz). Thus, an "on" segment has a square-wave voltage applied which is 180 degrees out of phase with the signal on the back electrode; an "off" segment is in phase with the back electrode. Because of their relatively slow turn-on characteristic, LCD's are usually not multiplexed, and a separate connection is required for each segment; the back electrode is common.

COS/MOS LCD Drivers

RCA COS/MOS liquid-crystal-display drivers have internal level shifting (for use in applications where the logic level is not at the same potential as that required by the display), latching, and BCD decoding.

The CD4055 and CD4056 are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip, as shown in Fig. 167. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signal swing (V_{DD} to V_{SS}) may be as low as 0 to -3 volts, while the output-display drive-signal swing (V_{DD} to V_{EE}) may be from 0 to -15 volts. If V_{DD} to V_{EE} exceeds 15 volts, V_{DD} to V_{SS} should be at least 4 volts.

The 7-segment outputs are controlled by a square wave at the display-frequency (DF) input, as shown in Fig. 168. Selected segments have a square-wave output voltage that is 180 degrees out of phase with the DF

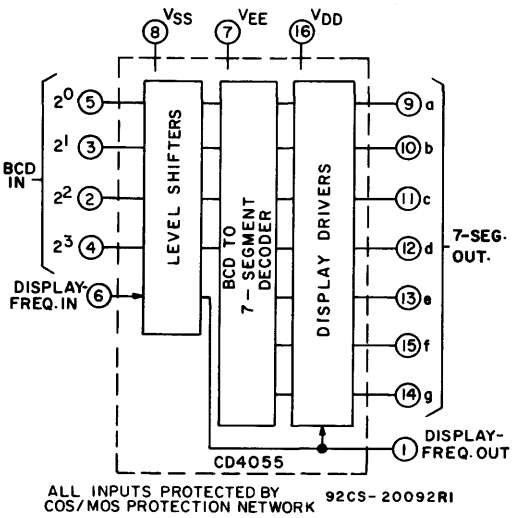


Fig. 167(a) — Functional diagram for the CD4055 liquid-crystal BCD-to-7-segment decoder/driver with "display-frequency" output.

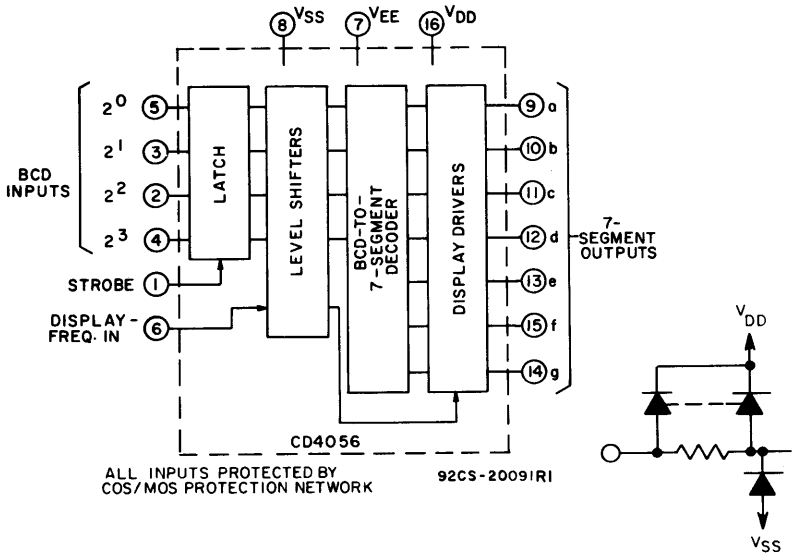


Fig. 167(b) – Functional diagram for the CD4056 liquid-crystal BCD-to-7-segment decoder/driver with strobed-latch function.

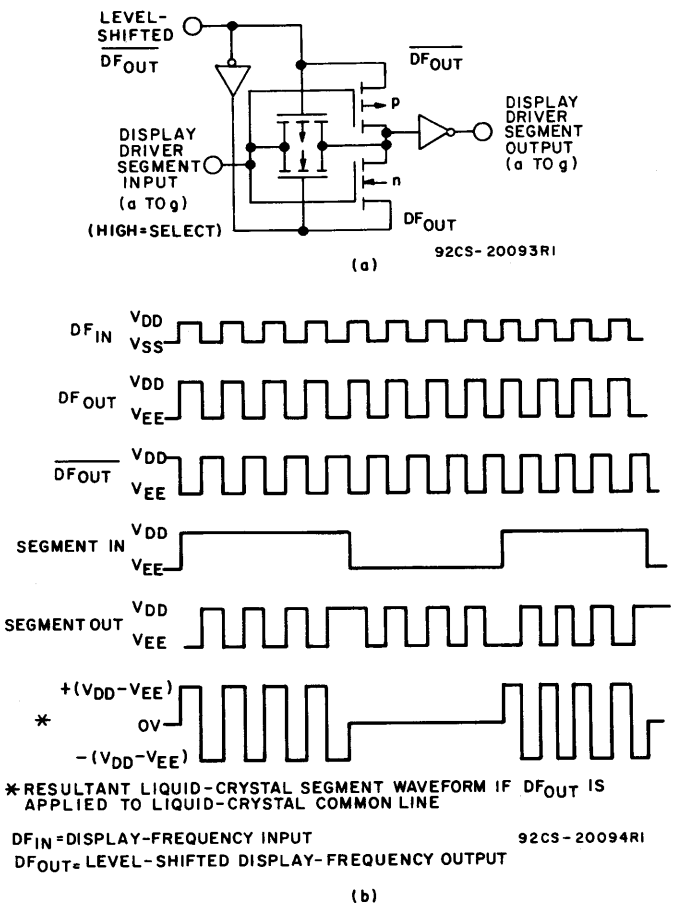


Fig. 168 – Display-driver circuit for one segment line and waveforms.

inputs; segments which are not selected have a square-wave output in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The CD4055 provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The CD4056 provides a strobed-latch function at the BCD inputs.

The truth table for the CD4055 and CD4056 is shown in Fig. 169. Decoding of all input combinations provides displays of 0 to 9, as well as L, P, H, A, -, and a blank position. Fig. 170 shows the use of the CD4055 in a typical circuit for a single-digit display.

The CD4054, shown in Fig. 171, provides level shifting similar to that of the CD4055 and CD4056, independently strobed latches, and common DF control on 4 signal lines. The CD4054 is intended to provide drive-signal compatibility with the CD4055 and CD4056 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any CD4054 output line by connecting the corresponding input and strobe lines to a low and high level, respectively.

The CD4054 may also be used for logic-level up-conversion and down-conversion.

INPUT CODE				OUTPUT STATE							DISPLAY CHARACTER
2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	
0	0	0	1	0	1	1	0	0	0	0	
0	0	1	0	1	1	0	1	1	0	1	
0	0	1	1	1	1	1	1	0	0	1	
0	1	0	0	0	1	1	0	0	1	1	
0	1	0	1	1	0	1	1	0	1	1	
0	1	1	0	1	0	1	1	1	1	1	
0	1	1	1	1	1	1	0	0	0	0	
1	0	0	0	1	1	1	1	1	1	1	
1	0	0	1	1	1	1	1	0	1	1	
1	0	1	0	0	0	0	1	1	1	0	
1	0	1	1	0	1	1	0	1	1	1	
1	1	0	0	1	1	0	0	1	1	1	
1	1	0	1	1	1	1	0	1	1	1	
1	1	1	0	0	0	0	0	0	0	1	
1	1	1	1	0	0	0	0	0	0	0	BLANK

Fig. 169 – Truth table for the CD4055 and CD4056.

For example, input-signal swings (V_{DD} to V_{SS}) from 5 volts to 0 can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 volts to -5 volts.

The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD}, while the output swings from a low level of V_{EE} to the same high level of V_{DD}. Thus the input and output swings can be selected independently of each other over a 3-to-18-volt range.

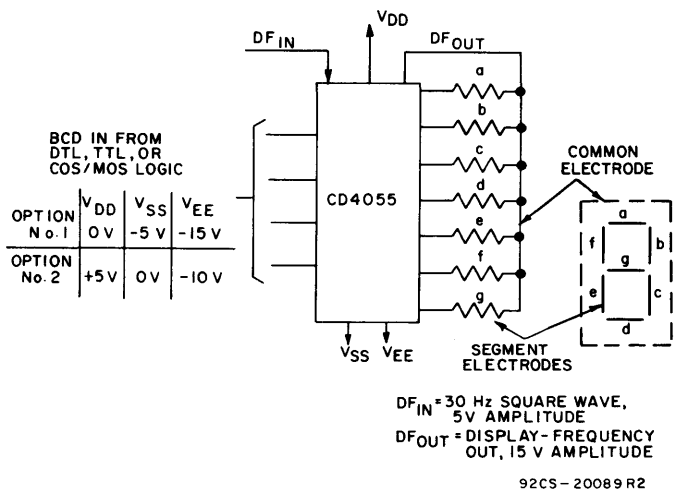


Fig. 170 – Single-digit liquid-crystal display.

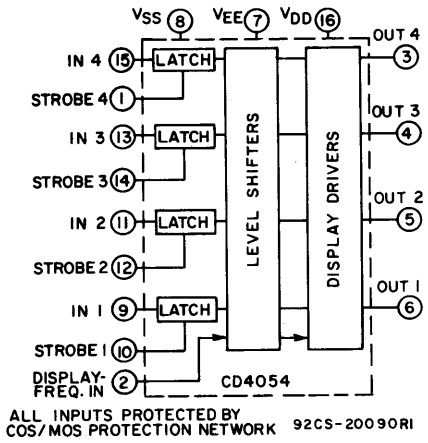


Fig. 171 – Functional diagram for the CD4055 4-line liquid-crystal-display driver.

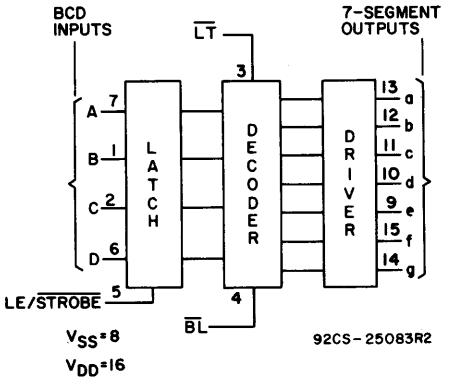


Fig. 172 – Functional diagram for the CD4511 latch decoder driver.

LIGHT-EMITTING-DIODE DISPLAYS

Light-emitting diodes (LED's) used in digital displays are usually gallium-arsenide-phosphide diffused planar devices. Their extremely fast response time allows them to be multiplexed and thus reduces interconnection wiring. Multiplexing, however, requires an increase in the pulsed current by a factor equal to the duty cycle.

In an eight-digit display, for example, each digit is driven only one-eighth of the time. To maintain equivalent brightness, therefore, a segment with an average dc current requirement of 3 milliamperes must be pulsed with 24 milliamperes. Sourcing currents of this magnitude are not practicable with conventional COS/MOS geometries.

Fig. 172 shows the functional diagram of the CD4511 latch decoder driver, which combines bipolar n-p-n transistor output devices with COS/MOS logic in a single monolithic structure. The COS/MOS logic includes a BCD latch and a BCD-to-7-segment decoder; the bipolar devices in the driver stage can source up to 25 milliamperes. This capability allows the CD4511 to drive LED's, incandescent displays, and low-voltage fluorescent displays directly.

The truth table for the CD4511 is shown in Fig. 173, and its logic diagram in Fig. 174.

LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X ≡ Don't Care

* Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).

Fig. 173 – Truth table for the CD4511.

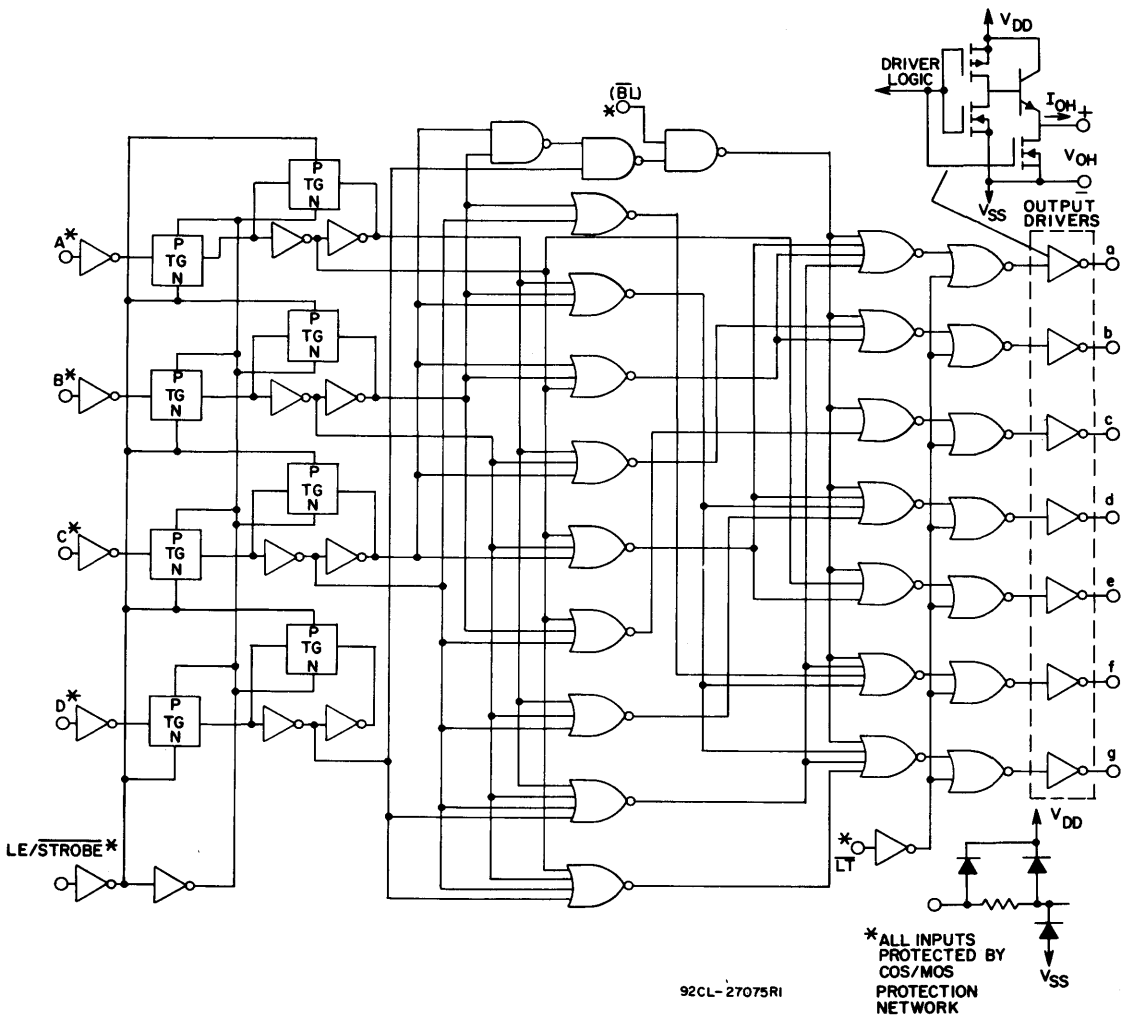


Fig. 174 – Logic diagram for the CD4511.

X. Frequency Synthesizers

Digital frequency synthesizers using COS/MOS integrated circuits offer the communications equipment designer several advantages in comparison to techniques which employ tuned circuits and banks of quartz crystals. To begin with, they use digital MSI functions, which reduce cost and increase reliability and dissipate only nanowatt standby power and milliwatt operational power. In addition, they use a single crystal reference for all synthesized frequencies. Spurious signals and unwanted harmonics are reduced (yielding a cleaner waveform) by elimination of tuned circuits (resulting in lower manufacturing/test costs and less maintenance on equipment). Finally, a simplified manual control is achieved by replacement of complex, mechanical tuning mechanisms with simple digitally coded switches.

PHASE-LOCKED LOOP

The basic unit in any digital frequency synthesizer is the phase-locked loop (PLL). In its simplest form, this circuit consists of three parts: a phase comparator, a low-pass filter, and a voltage-controlled oscillator (VCO); all three are connected to form a closed-loop frequency-feedback system, as shown in Fig. 175.

When no input signal is applied to the PLL system, the tuning (error) voltage at the output of an edge-triggered phase comparator is zero. The voltage from the low-pass filter is at a value that causes the VCO to operate at the minimum design frequency, f_{min}.

When a reference input signal is applied to the PLL, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage proportional to the phase and frequency difference of the input signal and the VCO. The error voltage, which varies in a direction that reduces the frequency difference between the VCO and the reference signal frequency, is filtered and applied to the control input of the VCO.

When the VCO frequency is sufficiently close to the reference frequency, the closed-loop nature of the PLL forces the VCO to lock in frequency with the input signal; i.e., when PLL is in lock, the VCO frequency is identical to the input signal except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the lock range of the system. The lock range is always greater than or equal to the bank of frequencies over which the PLL can acquire a locked condition with the input signal. This latter band of frequencies is defined as the capture range of the PLL system.

In practical digital phase-locked-loop systems, the VCO output frequencies are higher than the reference frequency.

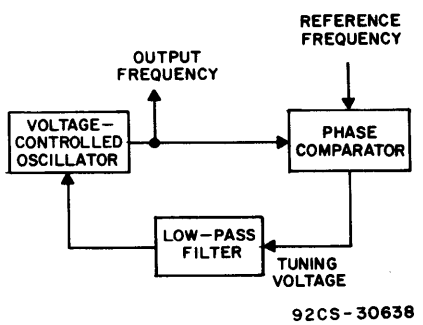


Fig. 175 – Basic digital phase-locked loop.

Addition of a divide-by-N counter between the VCO and the phase comparator, as shown in Fig. 176, permits selection of a wide

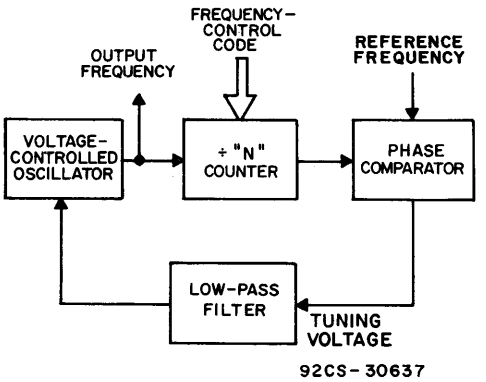


Fig. 176 – Typical digital phase-locked loop.

range of VCO frequencies, dependent on the programmed counter setting. In this case, the VCO locks at a frequency which is the product of the reference frequency and the countdown factor.

The CD4046 COS/MOS micropower phase-locked-loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-volt zener diode is provided for supply regulation if necessary. A block diagram of the CD4046 is shown in Fig. 177.

VCO Section

The VCO requires an external capacitor (C1) and one or two external resistors (R1, or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO, and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance (10^{12} ohms) of the VCO simplifies the design of low-pass filters by permitting a wide choice of resistor-to-capacitor ratios. A source-follower output of the VCO input voltage is provided at terminal 10 (demodulated output) to prevent loading of the low-pass filter. If terminal 10 is used, a load resistor (R_S) of 10 kilohms or more should be connected from terminal 10 to V_{SS}. If it is not used, terminal 10 should be left open.

The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The full COS/MOS logic swing available at the output of the VCO allows direct coupling to COS/MOS frequency dividers such as the CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. The CD4046 phase-locked-loop can be used in combination with one or more CD4018 presettable divide-by-N counters, or CD4029 presettable up/down counters, or CD4059 programmable divide-by-N counters, or CD40192/CD40193 presettable up/down counters to build a

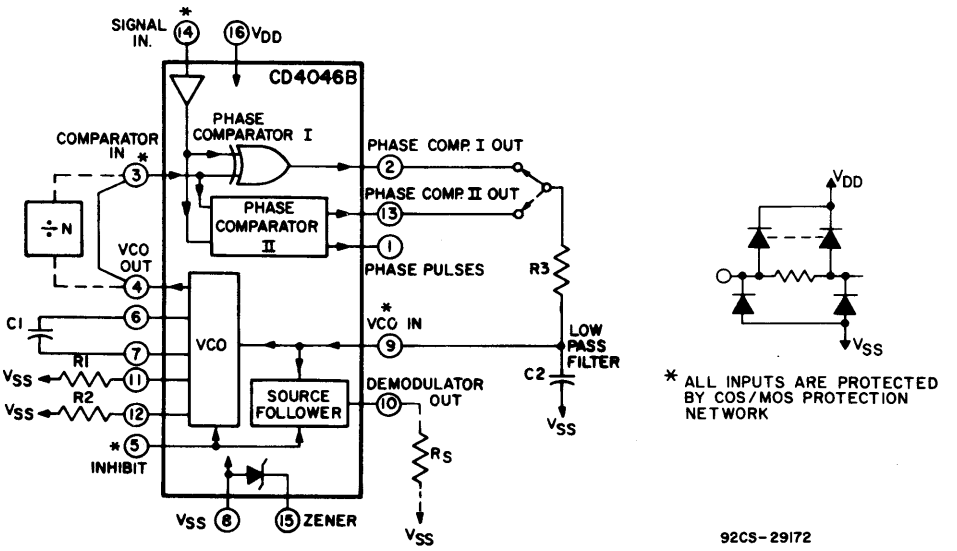


Fig. 177 – Block diagram of CD4046 COS/MOS micropower phase-locked loop.

micropower low-frequency synthesizer. A logic "0" on the inhibit input enables the VCO and the source follower; a logic "1" turns off both to minimize standby power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels, i.e., logic "0" $\leqslant$ 30% (V_{DD} - V_{SS}), logic "1" $\geqslant$ 70% (V_{DD} - V_{SS}). For smaller swings, the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analogously to an overdriven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50-per-cent duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the average voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_0).

The frequency range of input signals on which the PLL will lock if it is initially out of lock is defined as the frequency capture range ($2f_c$). The frequency range of input signals on which the loop will stay locked if it is initially in lock is defined as the frequency lock range ($2f_L$). The capture range is equal to or less than the lock range.

With phase comparator I, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass-filter characteristics, and can be made as large as the lock range. Phase comparator I permits a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0 and 180 degrees, and is 90 degrees at the center frequency. Fig. 178 shows the typical triangular phase-to-output response characteristic of phase comparator I. Typical

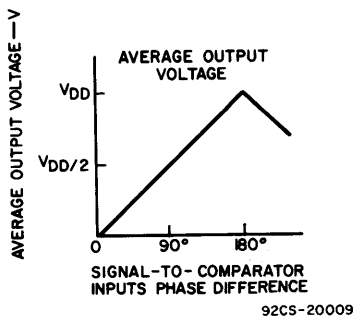


Fig. 178 – Characteristics of CD4046 phase comparator I at low-pass-filter output.

waveforms for a COS/MOS phase-locked loop employing phase comparator I in a locked condition of f_0 are shown in Fig. 179.

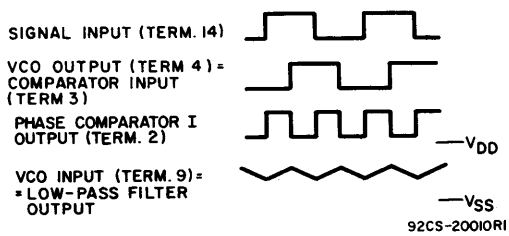


Fig. 179 – Typical waveforms for CD4046 with phase comparator I in locked condition f_0.

Phase comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers that have a common output node. When the p-MOS or n-MOS drivers are on, they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important because positive transitions control PLL systems that use this type of comparator.

If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained on most of the time, and both the n- and p-type drivers are off (3-state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained on most of the time, and both the n- and p-type drivers are off (3-state) the rest of the time. If the signal- and comparator-input frequencies are the

same, but the signal input lags the comparator input in phase, the n-type output driver is maintained on for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained on for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p- and n-type output drivers remain off, and thus the phase-comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant.

The signal at the "phase pulses" output is a high level most of the time. Small negative spikes, however, can be seen under normal locked conditions. This output can be used for indicating a locked condition when phase comparator II is used. For phase comparator II, therefore, no phase difference exists between signal and comparator input over the full VCO frequency range. In addition, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are off for most of the signal-input cycle.

It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 180 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

PROGRAMMABLE DIVIDE-BY-N COUNTER

The CD4059 is a divide-by-N down-counter that can be programmed to divide an input frequency by any number (N) from 3 to 15,999. The output signal is a pulse one-clock-cycle wide occurring at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down-counter is preset by means of 16 jam inputs. A functional block diagram of the CD4059 is shown in Fig. 181.

The three-mode-select inputs Ka, Kb, and Kc determine the modulus (divide-by number) of the first and last counting sections in accordance with the truth table shown in Fig. 182. Every time the first (fastest) counting section goes through one cycle, it reduces by one the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the divide-by-2 mode, only one flip-flop is needed in the first counting section. Therefore, the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If divide-by-10 is desired for the first section, Ka is set to 1, Kb to 1, and Kc to 0. Jam inputs J1, J2, J3, and J4 are used to preset the first counting section, and there

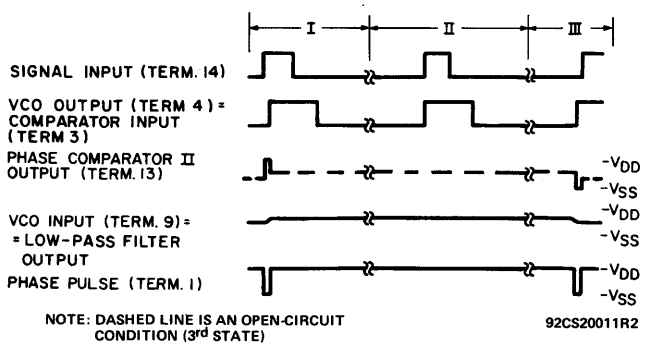


Fig. 180 – Typical waveforms for CD4046 with phase comparator II in locked condition.

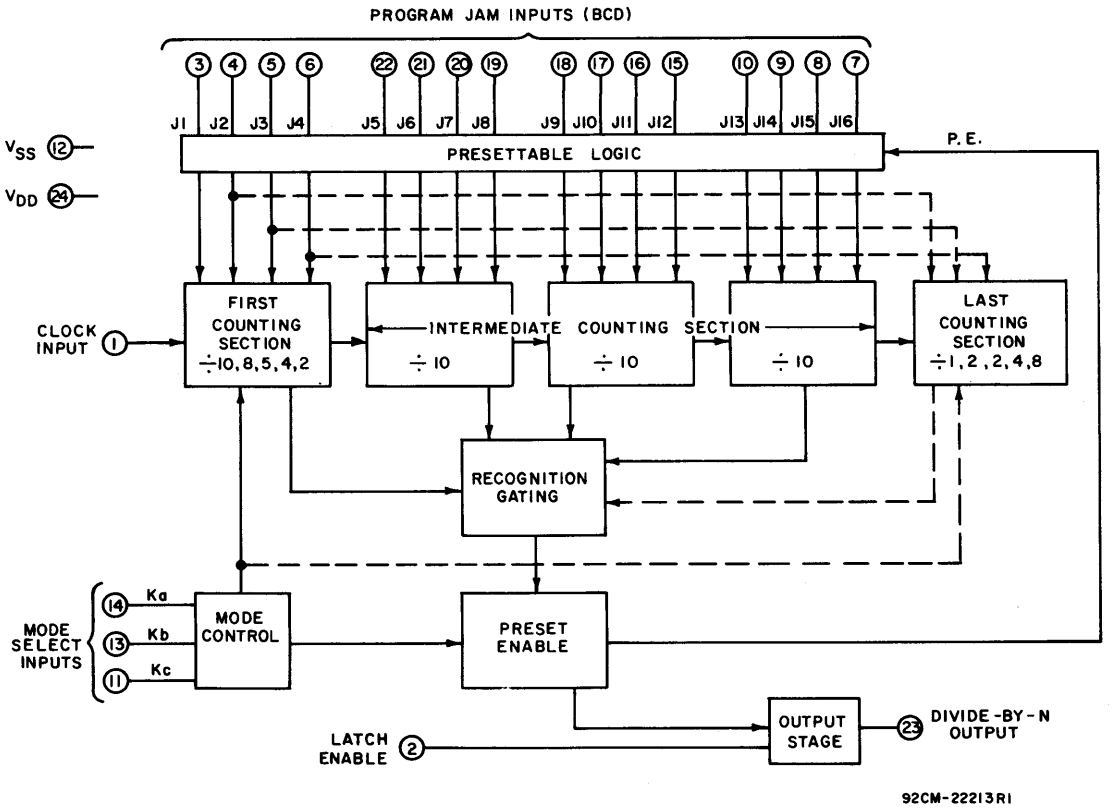


Fig. 181 – Functional block diagram for the CD4059 programmable divide-by-N counter.

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
									DESIGN	EXTENDED
Ka	Kb	Kc	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	Max.	Max.
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5#	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	–	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			–	–

X = Don't Care

▲ J1 = Least significant bit.
J4 = Most significant bit.

#Operation in the ÷5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, kc must be a logic "O" for a period of 3 input clock pulses after V_{DD} reaches a minimum of 3 volts.

Fig. 182 – Truth table for CD4059.

is no last counting section. The intermediate counting section consists of three cascaded BCD decade (divide-by-10) counters presettable by means of jam inputs J5 through J16.

The mode-select inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts for divide-by-10, 8, 5, 4, or 2, respectively. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100 multiplied by the number of the divide-by-N mode. For example, in the divide-by-8 mode, the number from which counting-down begins can be preset to 15 for the first decade, 150 for the second decade, 1500 for the third decade, and 1000 for the last counting section. The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the divide-by-8 mode.

The highest count of the various modes is shown in the column entitled "Extended Counter Range" in Fig. 182. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition, the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected. Whenever the master preset mode is used, control signals Kb = 0 and Kc = 0 must be applied for at least three full clock pulses. A "1" on the latch enable input will cause the counter output to remain in the high state after an output pulse cocurs until the latch input returns to "0". If the latch enable is "0", the output pulse will remain high for only one cycle of the clock-input signal.

After the Master Preset Mode inputs have been changed to one of the divide-by modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. After an MP (Master Preset) mode, therefore, there is always one extra count before the output goes high. Fig. 183 illustrates a total count of 3 for the divide-by-8 mode. Provided the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the proper time.

The CD4059 is particularly advantageous in communication digital frequency synthesis (VHF, UHF, FM, AM, etc.), where programmable divide-by-N counters are an integral part of the synthesizer phase-locked-loop subsystem. It can also be used to perform the synthesizer "Fixed Divide-by-R" counting function, and is useful in general-purpose counters for instrumentation functions such as totalizers, production counters, and "time-out" timers.

The CD4046 and CD4059 COS/MOS circuits can be used together to implement the system shown in Fig. 176. However, if the VCO output frequency exceeds the range of the CD4059 counter (3 MHz at 10 volts, 1.5 MHz at 5 volts), a fixed counter must be used to "prescale" the VCO output down to a lower frequency, as shown in Fig. 184. The prescaler can be any high-frequency counter. The reference frequency f_r is normally equal to the channel spacing frequency f_c. When a prescaling counter is employed, however, the value of f_r must be reduced by a division by K (i.e., $f_r = f_c/K$).

Phase-comparator reference frequencies are normally in the 1-to-10-kHz range, while the frequency (f_x) of a highly stable crystal-controlled oscillator is usually in the 2-to-5-MHz range. For this reason, the divide-by-R

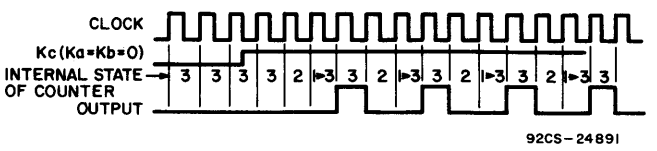


Fig. 183 – Waveforms for CD4059 in divide-by-8 mode for a total count of 3.

counter shown in Fig. 184 is used to reduce f_x by R (i.e., $f_r = f_x/R$).

RATE MULTIPLIERS

Rate multipliers are versatile MSI circuits that can be used as building blocks to generate a range of digital functions in various applications, such as frequency synthesis, digital filtering, and numerical control. When used with an up/down counter and control logic, they can perform such operations as multiplication, addition, subtraction, generation of algebraic equations, integration, and raising numbers to various powers.

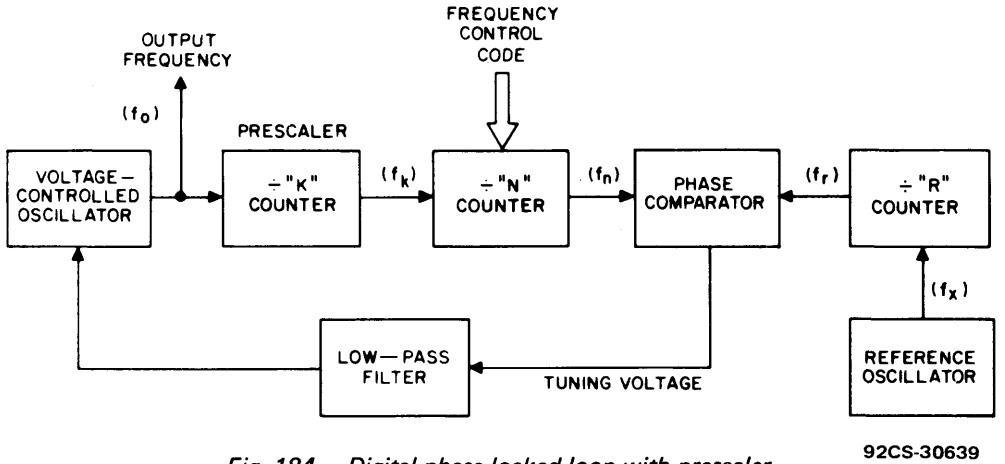


Fig. 184 – Digital phase-locked loop with prescaler.

The rate multiplier is a circuit that produces an output pulse train having a frequency proportional to the product of two inputs. One of the inputs is a clock frequency f_c, and the other a preprogrammed multiplier number (binary or BCD) with a fixed value at a given instant. The output of the rate multiplier is a frequency with an average rate equal to $f_c x$, where the value of x is between zero and unity. Thus, the output rate is always less than f_c, and is generally composed of pulses which are unevenly spaced. Even though the output rate is time-averaged to the correct fractional rate of the input, there is always a round-off error associated with the output. This error can be reduced by increasing the bit capacity of the multiplier.

The principle of rate multiplication can be illustrated by reference to the simplified circuit of a binary rate multiplier shown in Fig. 185. Four bits of binary information are used to perform multiplication by any factor from 1/16 to 15/16 by programming the S8, S4, S2, or S1 gates for the proper factor. The final output frequency f_x is obtained by OR-ing the outputs of each AND gate. The timing diagram in Fig. 186 shows how an output frequency f_x equal to (6/16) f_c can be obtained by gating the S4 and S2 outputs.

The CD4089 is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, and perform A/D and D/A conversions and frequency division. The functional and logic diagrams for the CD4089 are shown in Figs. 187 and 188.

For words of more than 4 bits, CD4089 devices may be cascaded in two different modes, Add and Multiply. Fig. 189 shows two CD4089's cascaded in the Add mode with a preset number of 189. In this mode, some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when the two units shown in Fig. 189 are programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13

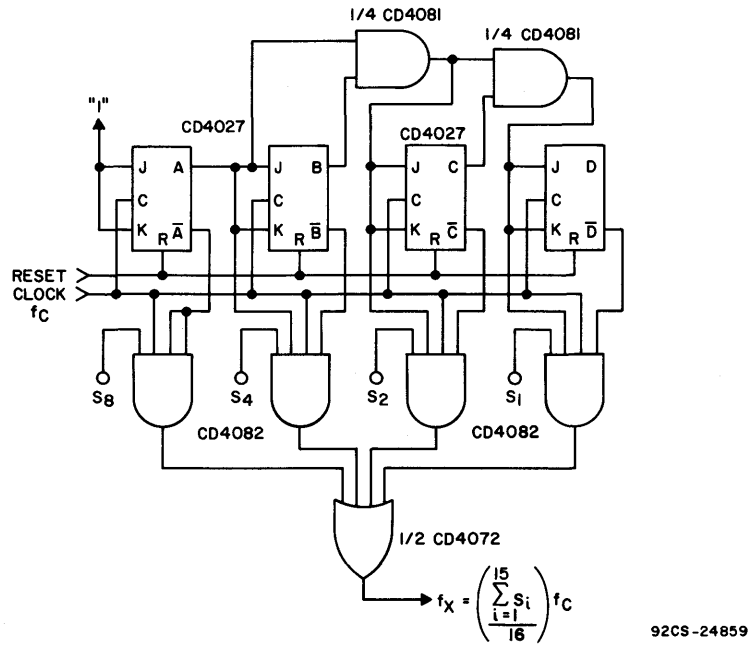


Fig. 185 – Simplified circuit of binary rate multiplier.

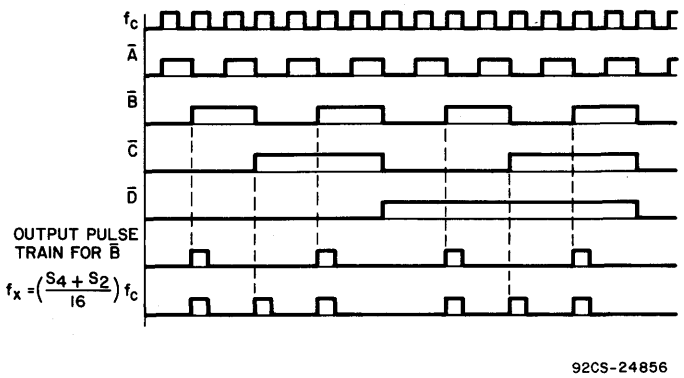


Fig. 186 – Timing diagram for circuit of Fig. 185.

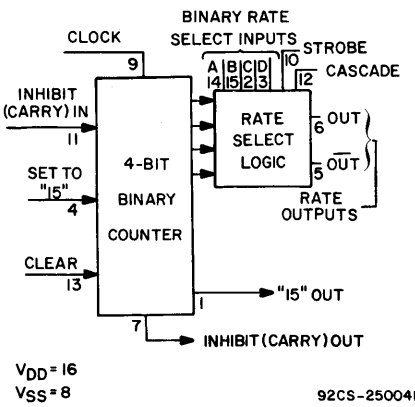


Fig. 187 – Functional diagram for CD4089 COS/MOS binary rate multiplier.

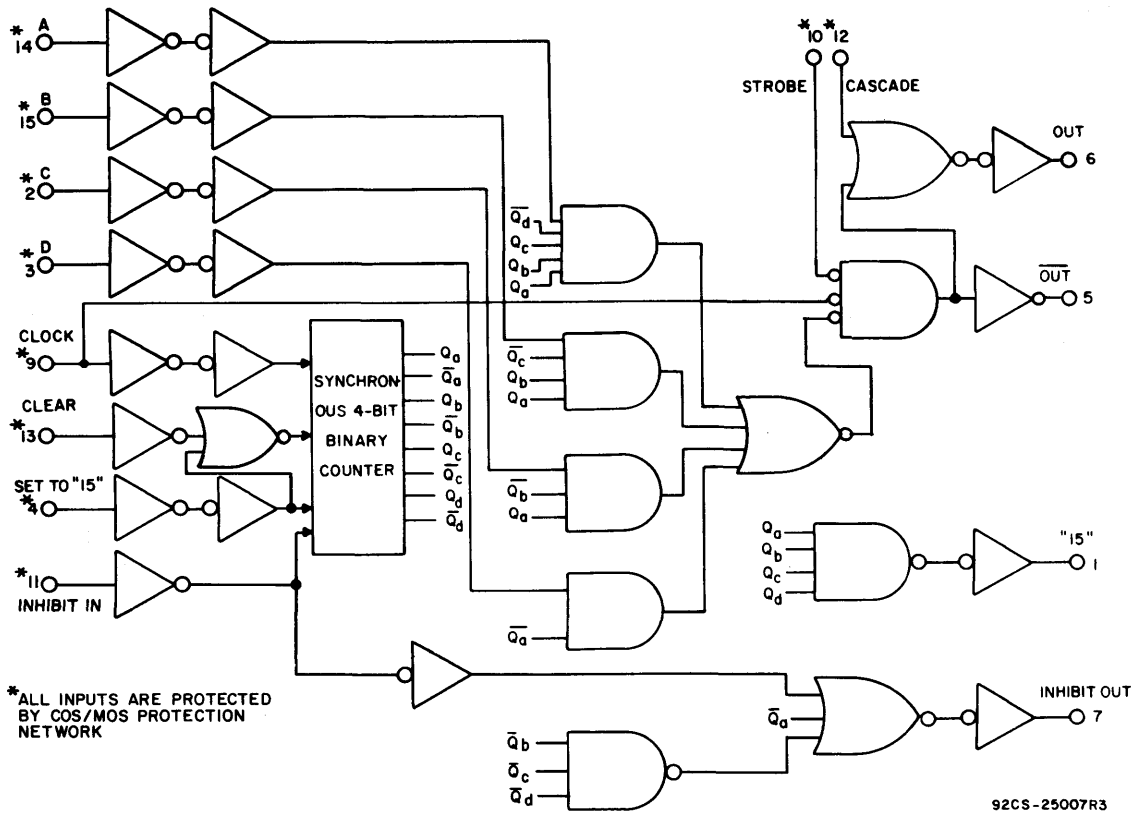


Fig. 188 – Logic diagram for CD4089 COS/MOS binary rate multiplier.

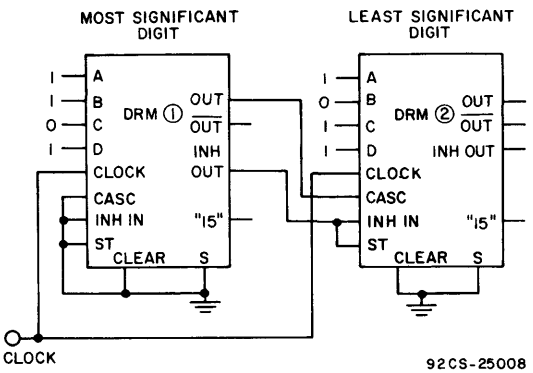


Fig. 189 – Two CD4089's cascaded in the Add mode with a preset number of 189.

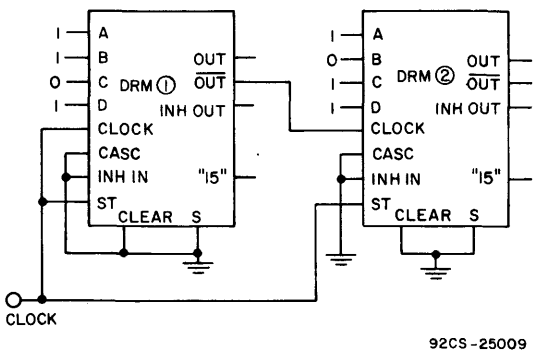


Fig. 190 – Two CD4089's cascaded in the Multiply mode with a preset number of 143.

output pulses for every 256 input pulses, for a total of

$$11/16 + 13/256 = 189/256$$

Fig. 190 shows two CD4089's cascaded in the Multiply mode with a preset number of 143. In this mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second rate multiplier. When the two units are programmed to 11 and 13, therefore, the output rate is

$$11/16 \times 13/16 = 143/256$$

The CD4089 has an internal synchronous 4-bit counter which, together with one of the

four binary input bits, produces pulse trains as shown in Fig. 191. If more than one binary input bit is high, the resulting pulse train is a combination of the separate pulse trains shown.

The CD4527 is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. Circuits which use this device perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, and perform A/D and D/A conversions and frequency dividion. The functional and logic diagrams for the CD4527 are shown in Fig. 192, and the timing diagram is shown in Fig. 193.

For fractional multipliers with more than one digit, the CD4527 devices may be cascaded in two different modes, Add and Multiply. Fig. 194 shows two CD4527's cascaded in the Add mode with a preset number of 94. In this mode, the BCD multiplier of each subsequent unit is one-tenth that of the preceding unit, i.e., the output rate equals ($0.1\ BCD_1 + 0.01\ BCD_2 + 0.001\ BCD_3 + \ldots$) times the clock rate. Therefore, if the two units in Fig. 194 are programmed to 9 and 4, respectively, the output rate is

$$9/10 + 4/100 = 94/100$$

or 94 output pulses for every 100 clock input pulses.

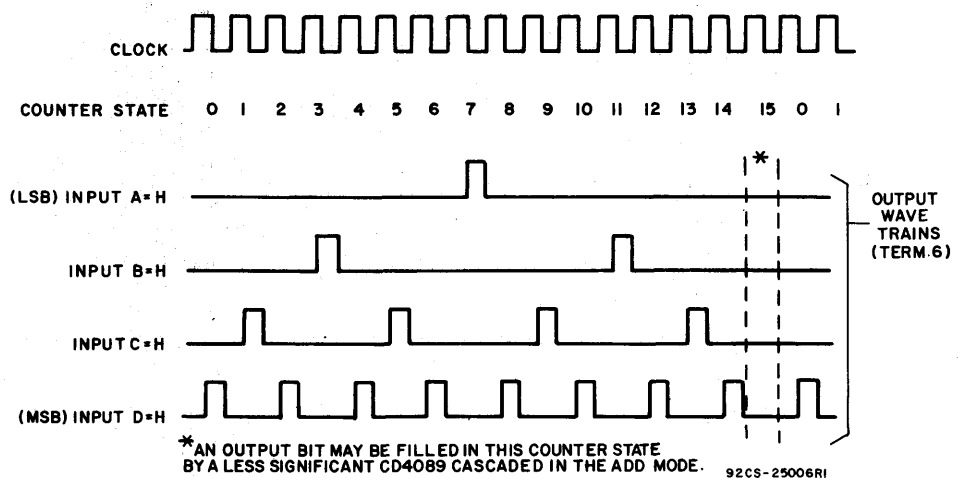


Fig. 191 – Timing diagram for CD4089 binary rate multiplier.

Fig. 195 shows two CD4527's cascaded in the Multiply mode with a preset number of 36. In this mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one. When the two units are programmed to 9 and 4, therefore, the output rate is

$$9/10 \times 4/10 = 36/100$$

or 36 output pulses for every 100 clock input pulses.

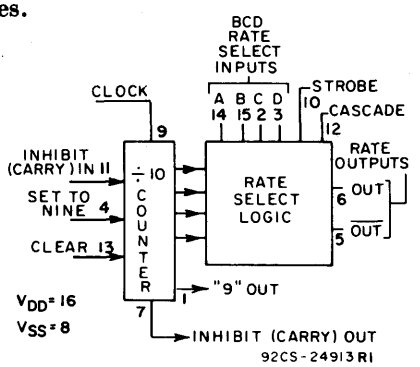


Fig. 192(a) – Functional diagram for the CD4527 BCD rate multiplier.

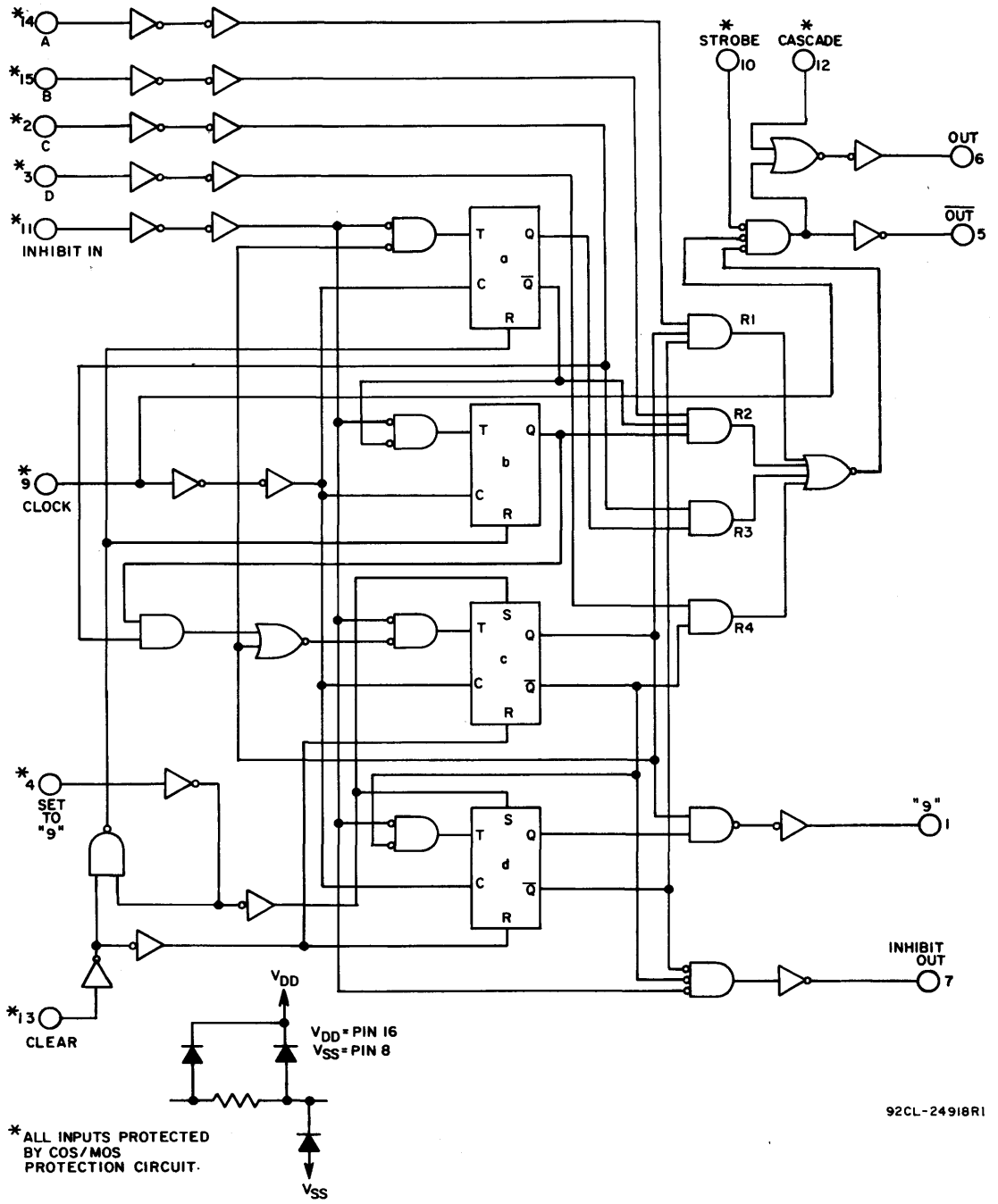


Fig. 192(b) – Logic diagram for the CD4527 BCD rate multiplier.

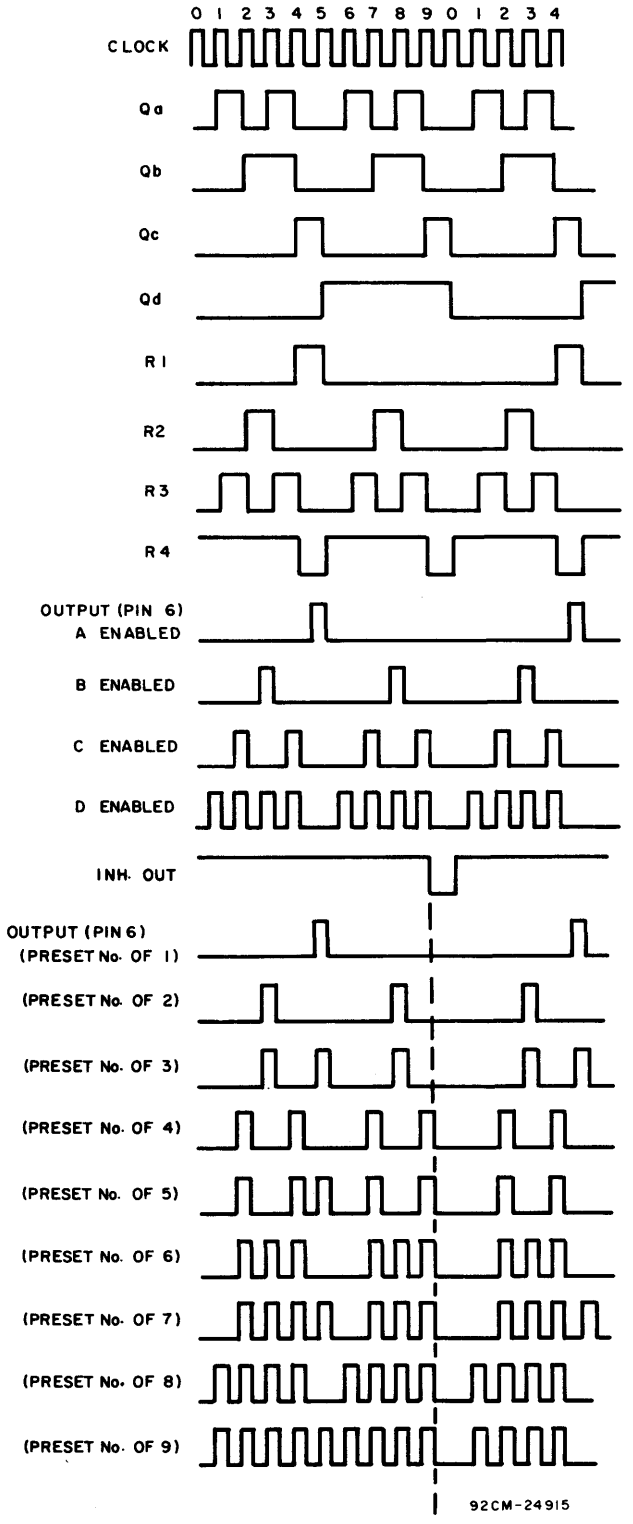


Fig. 193 – Timing diagrams for CD4527.

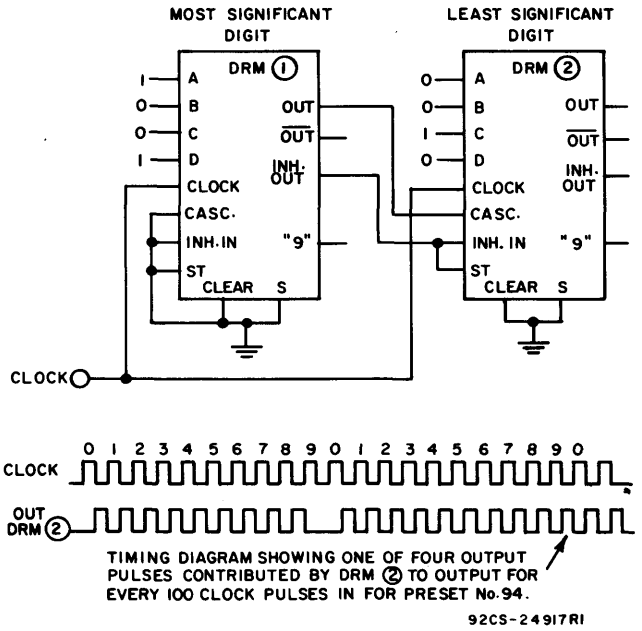


Fig. 194 – Two CD4527's cascaded in the Add mode with a preset number of 94.

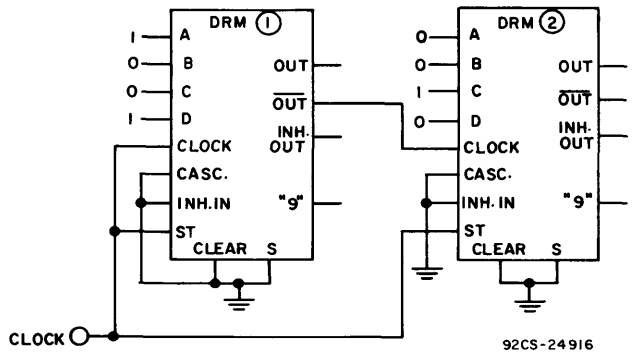


Fig. 195 – Two CD4527's cascaded in the Multiply mode with a preset number of 36.

XI. Introduction to Microprocessors and Memory Interfacing

The RCA CDP1802 is an LSI register-oriented COS/MOS microprocessor featuring an 8-bit parallel organization with bidirectional data bus, direct memory addressing up to 65,536 bytes (ROM/RAM), 91 instructions, DMA (direct memory access), a 16 x 16 register matrix, and ALU (arithmetic and logic unit). It utilizes the COSMAC architecture. The CDP1802 is designed for use as a general purpose computing or control element in a wide range of stored-program systems or products. Fig. 196 is a block diagram of a typical system using the CDP1802 microprocessor.

Under program control the CDP1802 can perform operations which include:

a) control of input/output (I/O) devices,
b) transfer of data or control information between I/O and memory (M),
c) movement of data bytes between different memory locations,
d) interpretation or modification of bytes stored in memory.

The COSMAC microprocessor has optional on-chip oscillator circuitry. The selection of crystal or RC oscillator frequency determines the time for each machine cycle. (Each machine cycle consists of eight clock pulses; each instruction requires two or three machine cycles. Thus, with a clock frequency of 6.4 MHz, each machine cycle would be

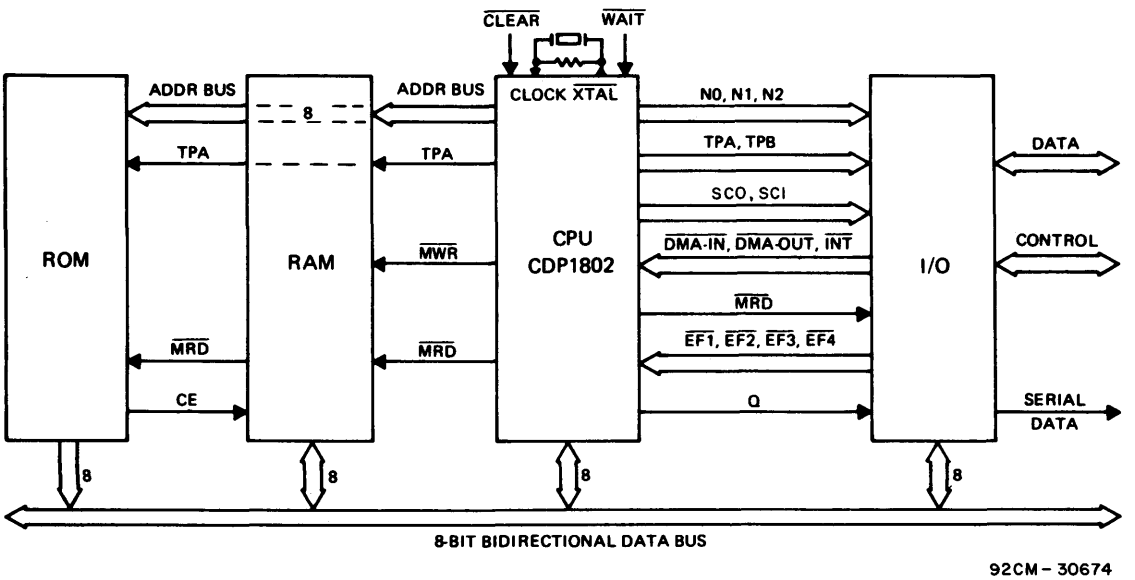


Fig. 196 – Block diagram of typical computer system using the RCA COSMAC Microprocessor CDP1802.

1.25 microseconds, and instructions would be executed in 2.5 to 3.75 microseconds, depending on the instruction.).

COSMAC MICROPROCESSOR INTERNAL STRUCTURE

The COSMAC architecture, Fig. 197, is based on a register array comprising sixteen general purpose 16-bit scratch-pad registers (R(n)), each holding two 8-bit bytes. A 4-bit binary code is used to designate each R scratch-pad register. Three 4-bit registers, labeled N, P, and X, hold the 4-bit binary codes that are used to select individual 16-bit scratch pad registers.

Memory or I/O data used in various COSMAC operations are transferred by means of the common, bidirectional 8-bit, data bus. Memory cycles involve both an address and the data byte itself. Memory addresses are provided by the contents of scratch-pad registers, via 16-bit register A. Register A is used to sequentially place the 16 memory address bits on the 8-bit memory address line, 8 bits at a time.

Either 8-bit byte in a scratch-pad register can be gated to the data bus for subsequent transfer to the 8-bit D register.

The 8-bit ALU performs arithmetic and logical operations. The byte stored in the D register is one operand, the byte on the bus (obtained from memory) is the second operand. The resultant byte replaces the operand in register D. A single-bit Data Flag indicates carry results from an add or shift operation. Two 4-bit registers I and N contain instruction bytes which operate on the Control Logic portion of the CDP1802.

The CDP1802 microprocessor has been designed to minimize external control circuitry, but some additional devices are necessary to provide gating, latching, and I/O (Input/Output) control. Standard parts from the CD4000 series discussed in this manual can be used to provide many of the systems operations; in addition, a growing family of RCA1800 series devices have been designed specifically to interface with the CDP1802.

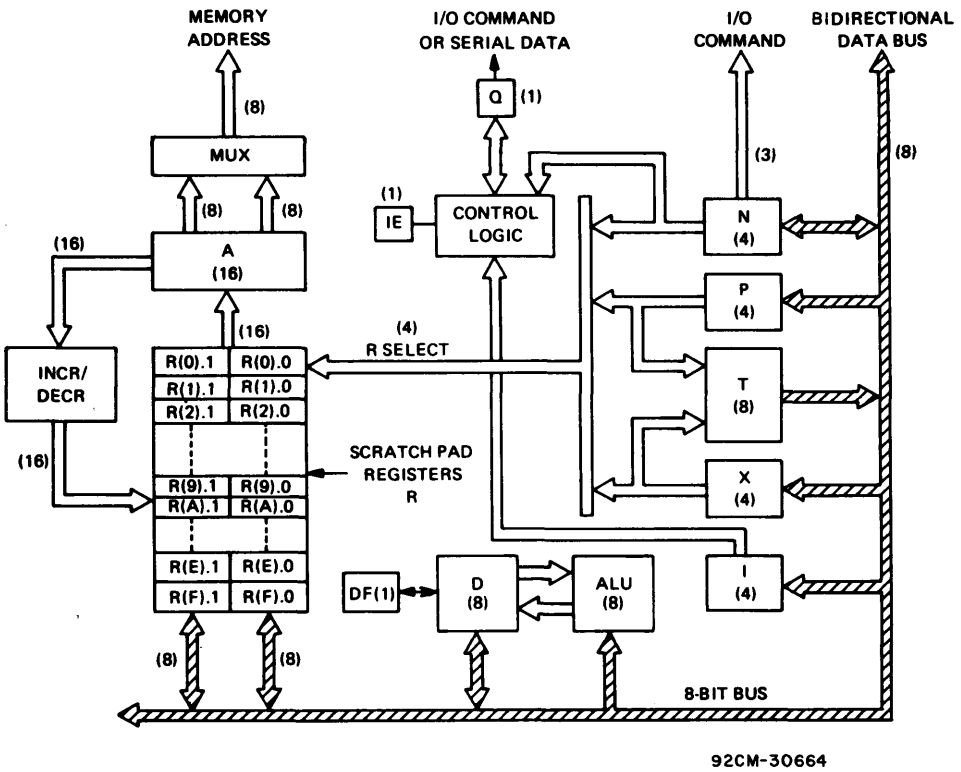


Fig. 197 – Internal structure of the CDP1802 microprocessor.

Fig. 198 shows one circuit, using standard devices from the CD4000 series, for controlling the run and load modes of the CDP1802. It includes a power-on reset feature.

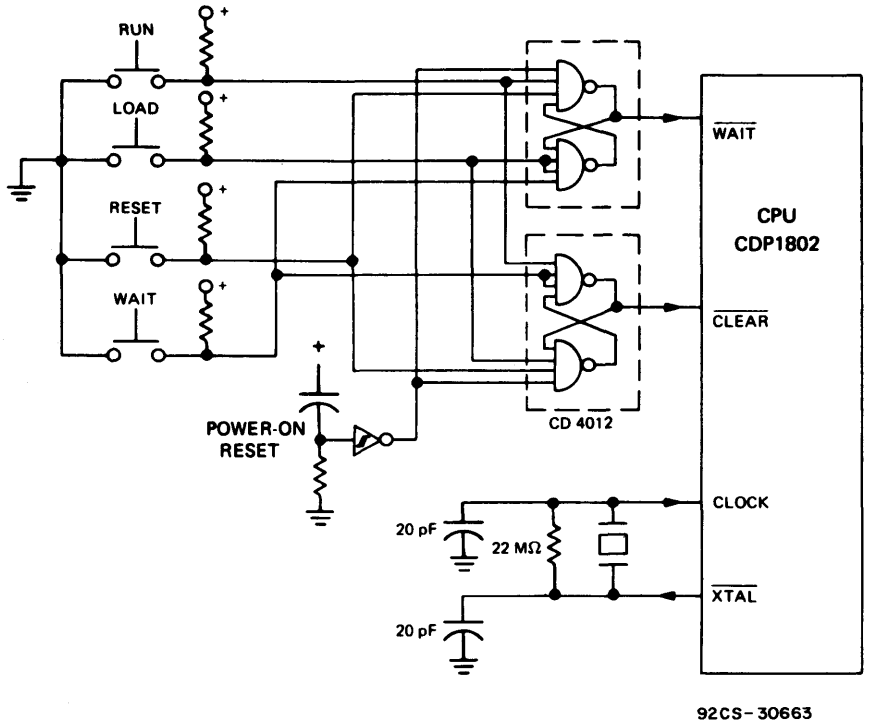


Fig. 198 – Simple control interface for CDP1802 microprocessor.

During normal operation, the $\overline{\text{CLEAR}}$ and $\overline{\text{WAIT}}$ lines are both held high. A low level on the $\overline{\text{CLEAR}}$ line will put the machine into the reset mode with I, N, X, P, Q, Data Bus = 0, and IE = 1. Actually, X, P, and R(0) are reset during a special S1 cycle (not available to the programmer) immediately following transition from the reset mode to any of the other modes (load, run, or pause). The clock must be running to effect this cycle.

If the $\overline{\text{CLEAR}}$ and $\overline{\text{WAIT}}$ lines are both held low, the machine enters the load mode. This mode allows input bytes to be sequentially loaded into memory beginning at M(0000). Input bytes can be supplied from a keyboard, tape reader, etc., by way of the DMA facility. This feature permits direct program loading without the use of external "bootstrap" programs in ROM's.

If the $\overline{\text{WAIT}}$ line is brought low (with $\overline{\text{CLEAR}}$ high), the CPU stops operation cleanly on the next negative-going transition of the clock (Pause mode). Output signals are held at their values indefinitely. This state is useful for several purposes. Using the $\overline{\text{WAIT}}$ line, the CPU can be easily single-stepped for debugging purposes or, if stopped early in the machine cycle, the CPU can be held off the data bus to allow for multiprocessor systems, etc. Also, the $\overline{\text{WAIT}}$ line can be used as a data-ready signal from a slow memory or peripheral, or signals TPA and TPB can be stretched. When the $\overline{\text{WAIT}}$ line is returned high, the machine resumes running on the next negative-going transition of the clock input. The $\overline{\text{WAIT}}$ signal does not inhibit the on-chip crystal oscillator. DMA's and Interrupts are not acknowledged in the Pause mode.

To load and start a program, the sequence of operations would be as follows: First, press the reset and then the load buttons. The CPU is now ready to load by means of the DMA channel. When loading is completed, pressing the reset and then the run buttons starts program execution at M(0000) with R(0) as the program counter (after one machine cycle). If a DMA request is present

when the run switch is turned on, the machine goes into the DMA state immediately with R(0) as the program counter. The user should therefore inhibit DMA externally until the program has changed to a program counter different from R(0). Interrupts, however, are disabled until the first instruction or DMA request is executed. This delay allows the programmer to place instruction 71 and 00 in the first two memory bytes to inhibit interrupts until he is ready for them. The combined effect of the two bytes is to set IE = 0. Interrupts must not occur, however, when the machine is in the load mode because they will force the machine into an an anomalous running state. Fig. 199 shows the sequence of events and states involved in loading a program via DMA-IN in the load mode and its subsequent execution. Fig. 200 provides a summary of the modes discussed, the control levels, and the characteristic features of these modes.

Another circuit that can be used for single-stepping the microprocessor (one machine cycle per switch depression) is shown in Fig. 201. This capability is often useful as a debugging aid.

External Flag Lines

Four external flag lines ($\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$) are available on the CDP1802. These lines provide the simplest input to the microprocessor. A low on any flag line places it in its true state; short branch instructions allow programs to determine the states of these flag lines. If the signal to the CPU is initiated by a switch closure, a flip-flop should be used to eliminate switch bounce as

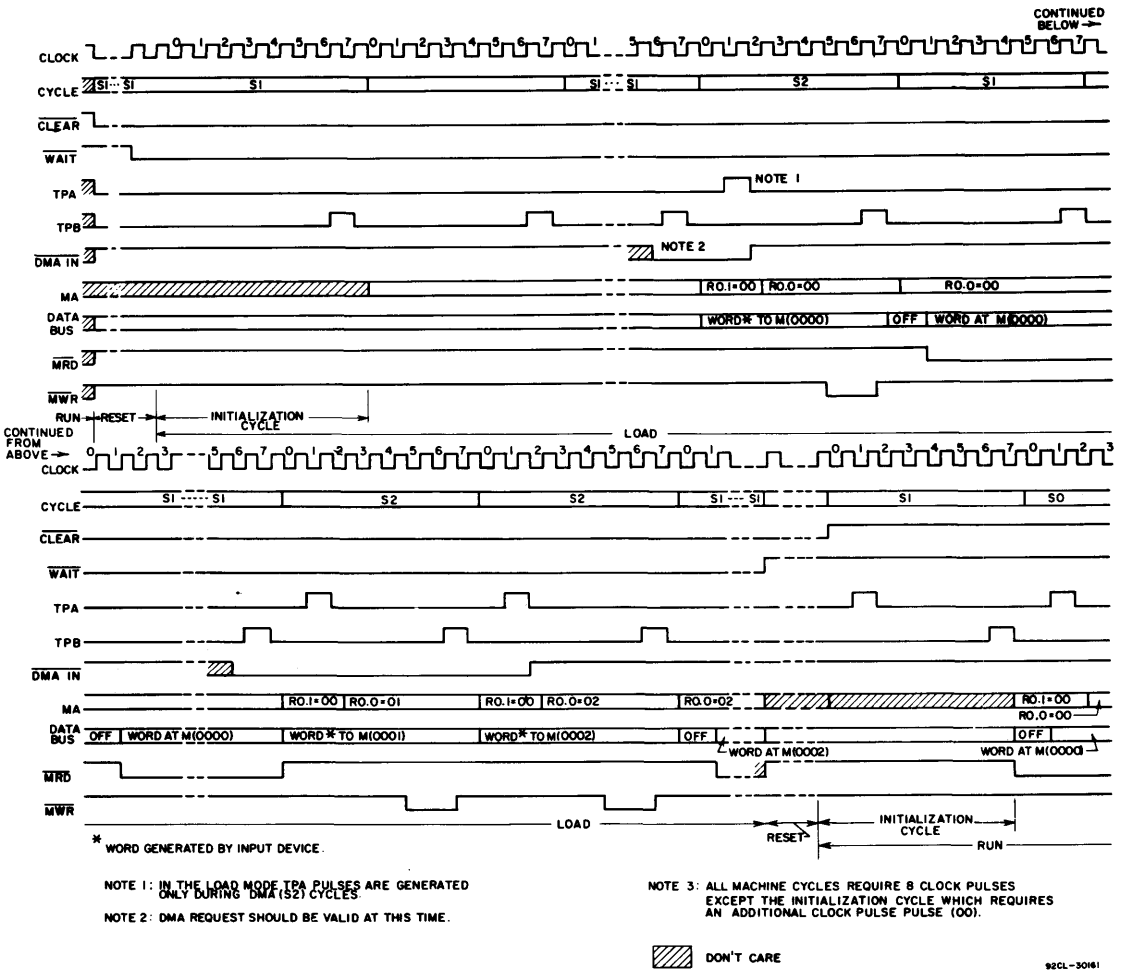


Fig. 199 — Timing diagram for load and run sequences.

MODE	$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	OPERATION
RESET	0	1	I, N, X, P = 0, R(0) = 0, Q = 0, BUS = 0, IE = 1; TPA and TPB are suppressed; CPU in S1.
RUN	1	1	CPU starts running one machine cycle after CLEAR is released. Execution starts at M(0000), or an S2 cycle follows if DMA was asserted. Internal sampling of interrupt is inhibited during initialization cycle.
RESET	0	1	As above.
LOAD	0	0	CPU in IDLE. An I/O device can load memory without "bootstrap" loader.
PAUSE	1	0	Clock: ⊓ ↓ ← stops internal operation. CPU outputs held indefinitely. Permits stretching of machine cycle to match slow devices or memory cycles. DMA and INTERRUPTS not acknowledged.
RUN	1	1	Clock: ⊓ ↓ - - - - - - - - - ⊓ Resume operation

Fig. 200 – Truth table for mode control of CDP1802 microprocessor.

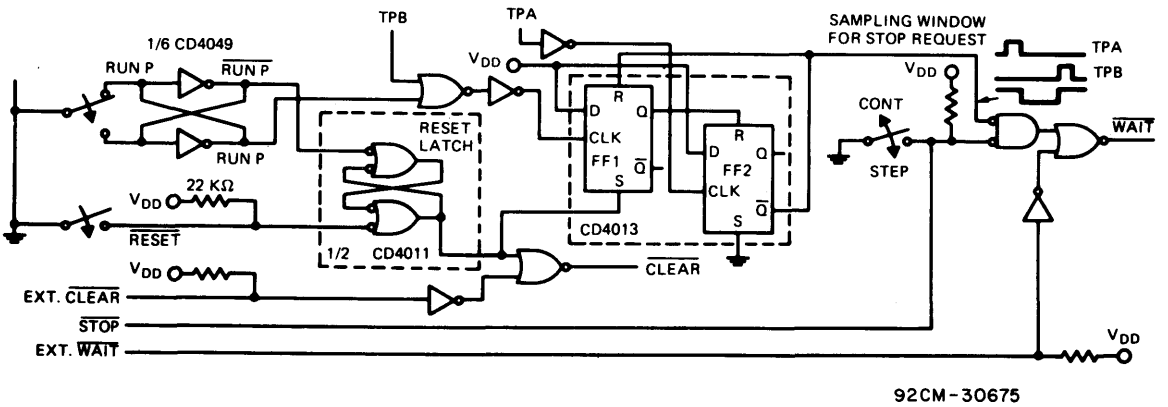


Fig. 201 – Circuit for single-stepping the CDP1802 microprocessor.

shown in Fig. 202. Also note the pull-up resistors, which prevent the gate inputs from floating in the "open" switch position.

OPERATION AND INTERFACING

Input/Output Port

The **RCA CDP1852** is a parallel, 8-bit, mode-programmable COS/MOS input/output port designed for use in RCA 1800 series microprocessor systems. It is compatible with and directly interfaces the CDP1802 without additional components. A functional diagram of the CDP1852 is given in Fig. 203.

The mode control is used to program the device as an input port (mode=0) or output port (mode=1). When the CDP1852 is used as an input port (mode=0), data is strobed into its 8-bit register by a high (1) level on the clock line. The negative, high-to-low transition of the clock sets the Service Request Flip-Flop ($\overline{SR}$=0) and latches the data in the register. The $\overline{SR}$ output can be used to signal the microprocessor. When CS1 · CS2=1 the three-state output drivers are enabled, the negative high-to-low transition of CS1 · CS2 resets the Service Request Flip/Flop, and $\overline{SR}$=1.

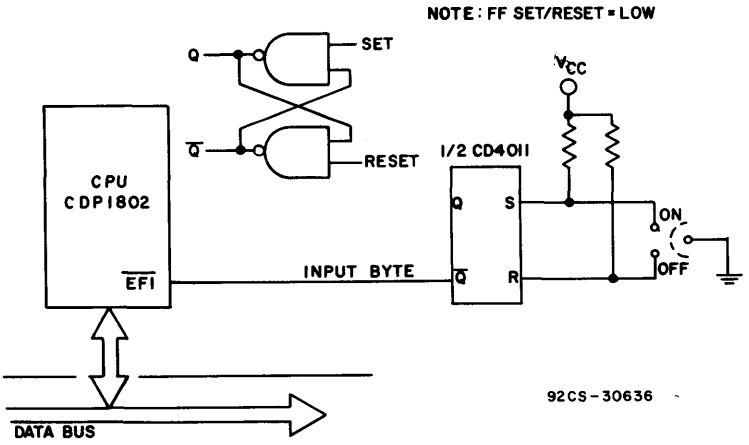


Fig. 202 – Use of a flag line (EF1) as an input command. Note flip-flop debounce circuit.

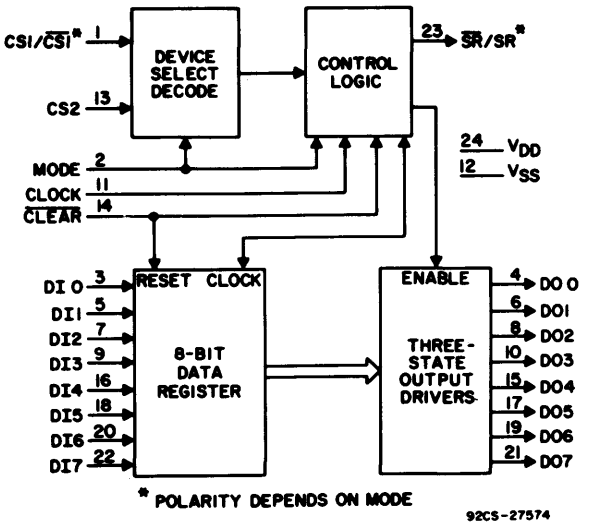


Fig. 203 – Functional diagram of CDP1852 input/output port.

If the CDP1852 is used as an output port (mode=1), data is strobed into the port's 8-bit register when $\overline{CS1} \cdot CS2 \cdot CLOCK=1$. The three-state output drivers are enabled at all times when the CDP1852 is configured as an output port. The service request signal is generated at the termination of $\overline{CS1} \cdot CS2=1$ and will be present, 1 level, until the following negative, high-to-low transition of the clock.

A $\overline{CLEAR}$ control is provided for resetting the port's register and service request flip-flop.

Fig. 204 shows the CDP1852 connected as part of a microprocessor system. The CDP-1852 can also be used as an address latch to demultiplex the CDP1802 address bus.

Display Output

Fig. 205 shows how an output instruction might be used to set a byte into a two-digit output LED display device. During the execution cycle of the instruction, when the N0 bit is valid, TPB will strobe valid data into the two BCD-to-7-segment latch decoder drivers.

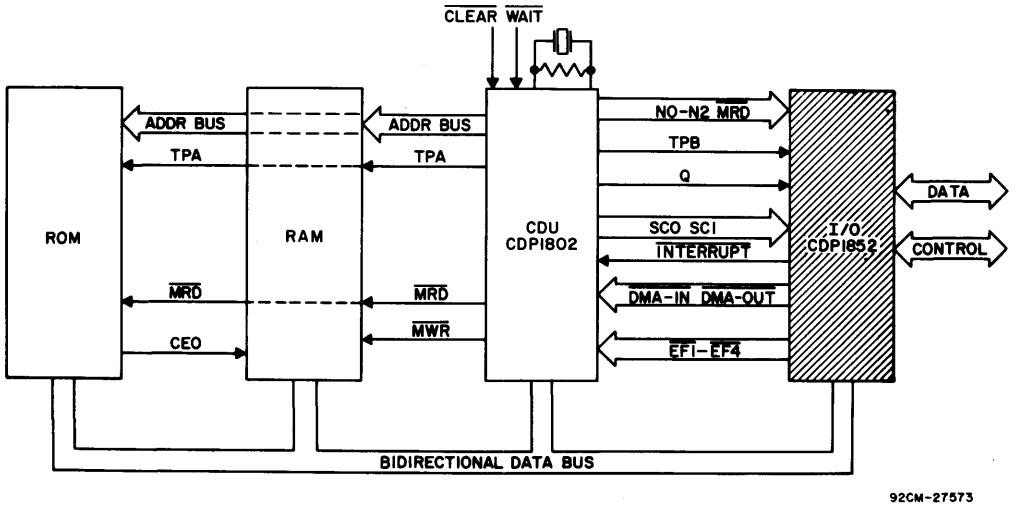


Fig. 204 – Typical CDP1802 microprocessor system showing CDP1852 used as I/O port.

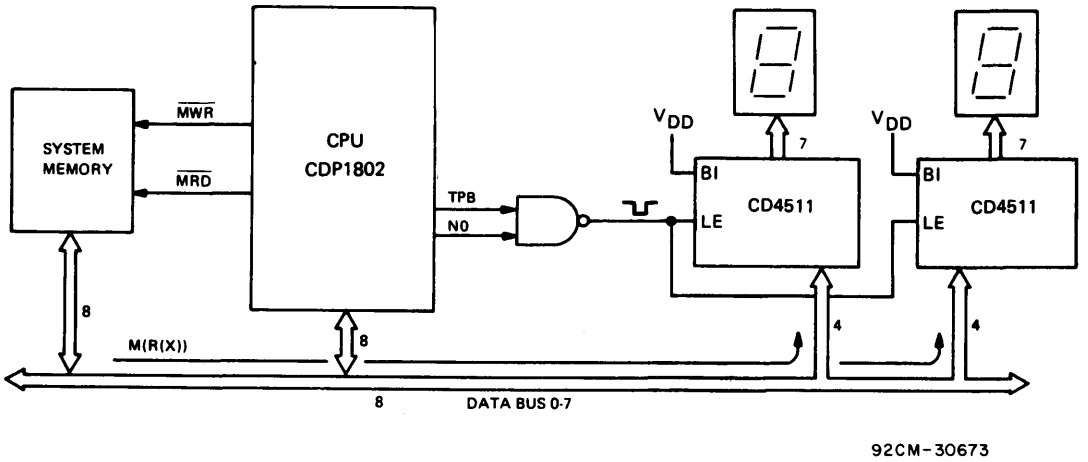


Fig. 205 – Direct selection of I/O devices—one pair of output display digits.

DMA Operation

The CDP1802 has a built-in direct memory access (DMA) facility which permits high-speed I/O byte transfer operations independent of normal program execution. Two lines, $\overline{\text{DMA-IN}}$ and $\overline{\text{DMA-OUT}}$, are used to request DMA byte transfer to and from the memory. A specific code is provided on the state code line (SC0,SC1) to indicate a DMA cycle. In Fig. 206, the CD4076 is used as a holding register (the CD4076 types are 4-bit, D-type registers that feature three-state outputs thus permitting isolation from the Data Bus line) and a CD4013 flip-flop is used to clock and hold the DMA request.

Fig. 206(a) illustrates the manner in which DMA-IN might be implemented. The leading edge of an enter pulse clocks an input byte into the register and activates the $\overline{\text{DMA-IN}}$ request.

Serial Interfacing

Fig. 207 shows the **CDP1854**, a CMOS Universal Asynchronous Receiver-Transmit-

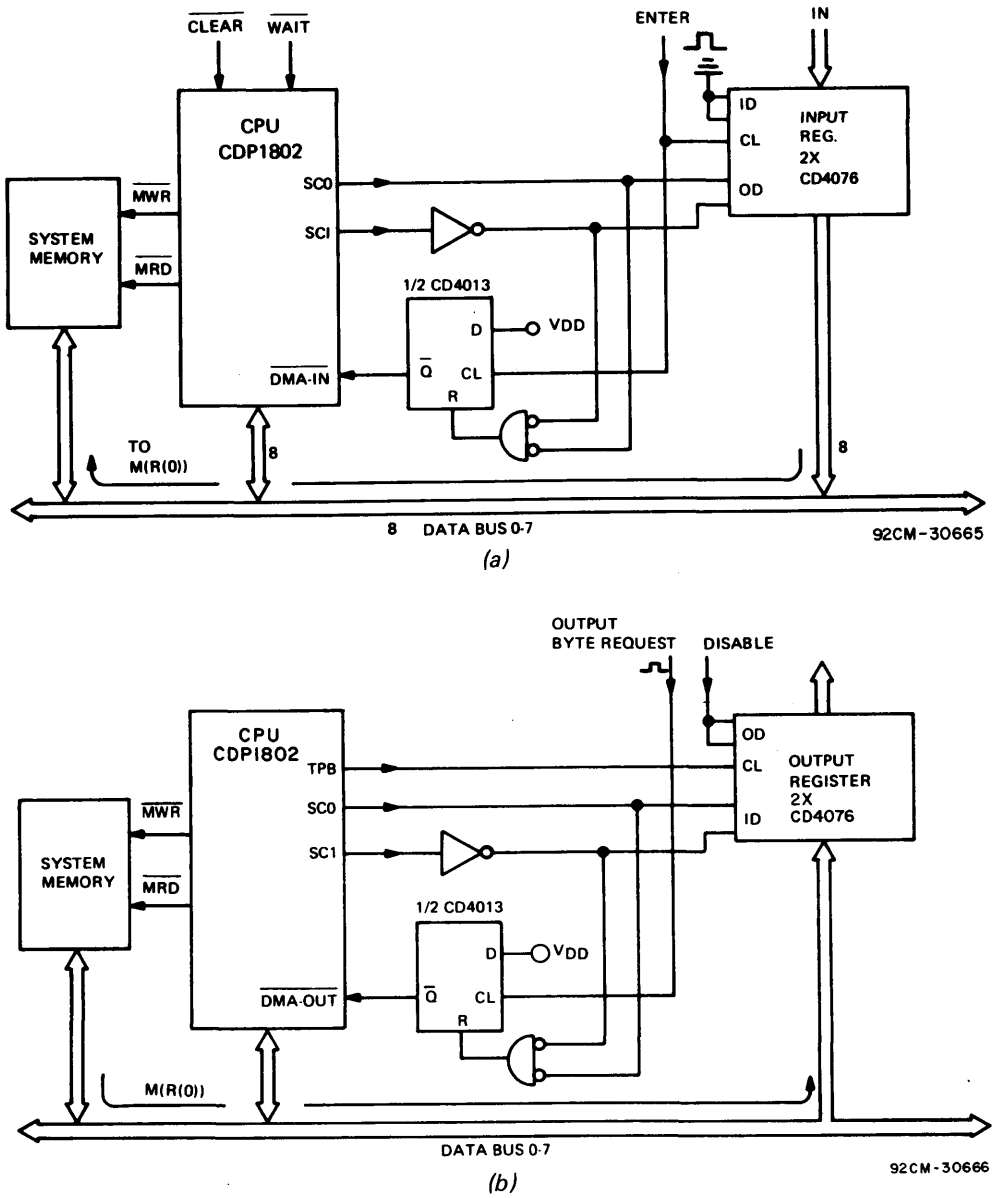


Fig. 206 – Implementation of DMA operation (a) DMA-IN (b) DMA-OUT.

ter (UART), interfaced to the CPU in a typical data communication application. The UART consists of a receiver and transmitter designed to provide the necessary formatting and control for interfacing serial asynchronous data to and from peripheral devices. The receiver-transmitter is capable of full duplex operation and is externally programmable.

The transmitter converts parallel data to a serial word containing the data (5-8 bits), a start bit, a parity bit (optional), and stop bits (1, 1-1/2, or 2), as illustrated in Fig. 208. The receiver converts a serial input word with start, data, parity, and stop bits into parallel data. It verifies proper code by checking parity and the receipt of a valid stop

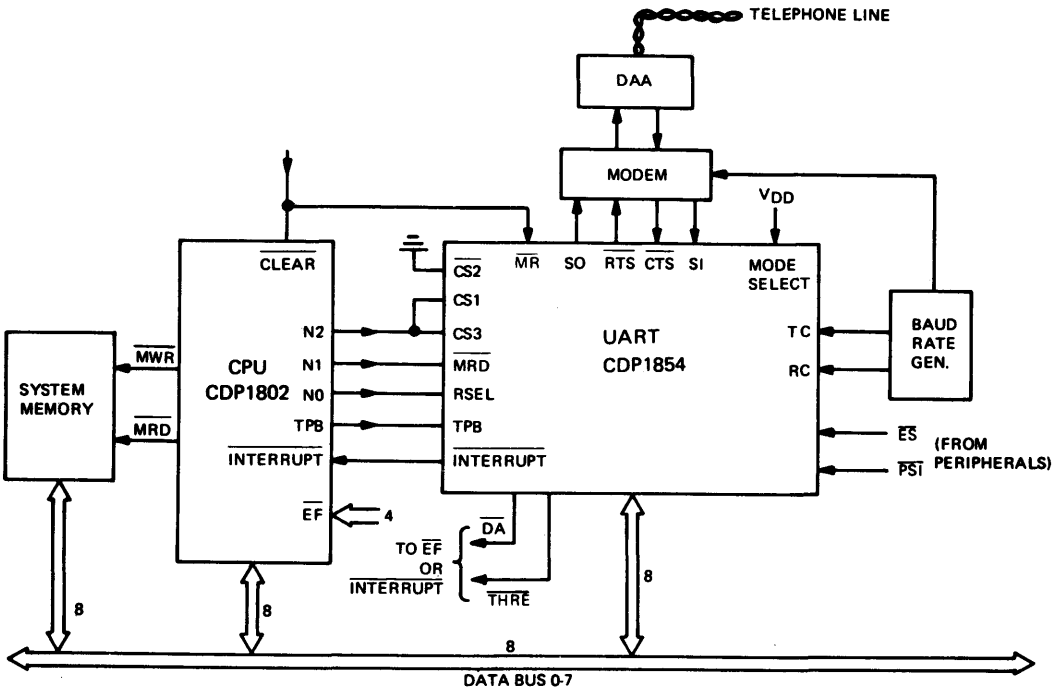


Fig. 207 – System configuration for asynchronous serial data communication interface.

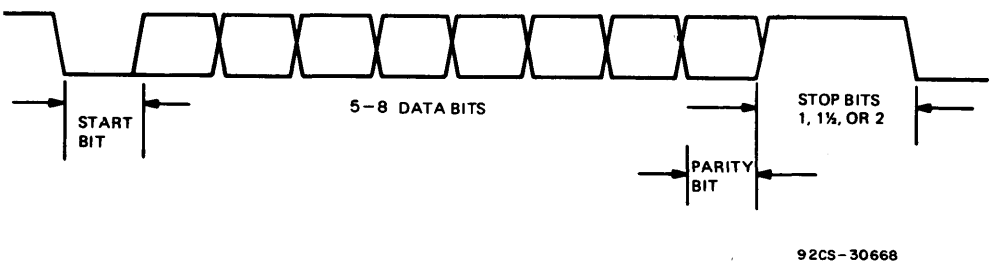


Fig. 208 – Word format in asynchronous serial data communications.

bit. Both the receiver and transmitter are double buffered.

Although the receiver and transmitter can operate with separate data buses, if the MODE SELECT line is high, the UART is directly compatible with the CDP1802 and bidirectional data transfer on a common bus.

There are four registers under program control in the UART. One is loaded from the bus in the transmit mode, one is read to the bus in the receive mode, a Control register is loaded from the bus at initialization, and a Status register is read in the receive mode. The two-bit code on $\overline{MRD}$ and RSEL determines which register is selected and the direction of data flow.

The UART is enabled to the data bus when the three chip selects are asserted. Therefore, by decoding, a large number of UART's can operate in a system on the same bus.

The CDP1802 can be programmed to emulate a general serial interface. In this configuration, the serial input is an external flag ($\overline{EF}_x$) and the serial output is Q.

Memory Interfacing

As shown in Fig. 209, up to 256 bytes of memory can be addressed directly by the CDP1802 through the memory interface lines, because only eight bits of address are required.

For larger memory systems, the addressing appears on the memory address lines in two bytes: first the high-order byte, which must be retained in a latch, then the low-order byte. Latching all eight bits in the high-order byte would provide for a memory of 65,536 bytes; chip select decoding would have to be added to the latch output.

Fig. 210 illustrates the interconnections of a static 4096-byte RAM to the CPU. Twelve memory address bits are required to select one out of 4096 memory byte locations. The high-order byte of a 16-bit memory address appears on the memory address lines first. The four least significant bits are strobed into the latch and decoder circuit CDP1858 by timing pulse TPA. The functional diagram for the CDP1858, a four-bit latch with decode designed for use with RCA1800 series microprocessor systems, is given in Fig. 211.

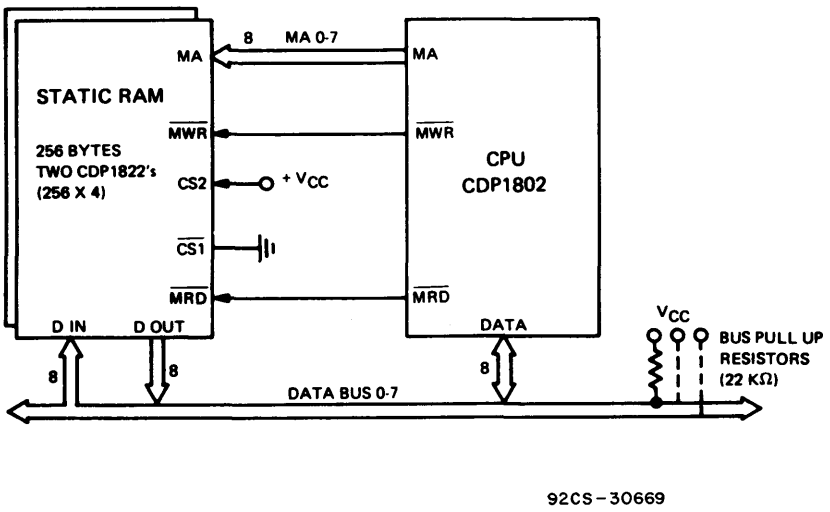


Fig. 209 – Interface for the CDP1822 static RAM to the CDP1802 microprocessor in a 256-byte RAM system.

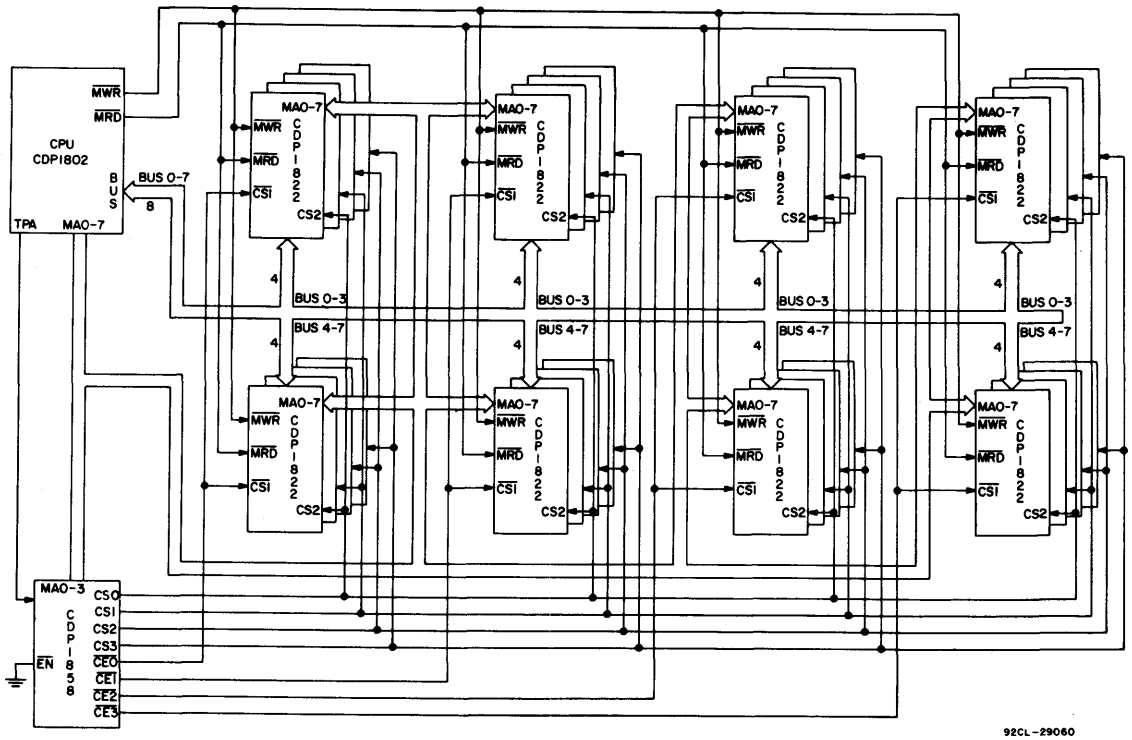


Fig. 210 – Interface for the CDP1822 static RAM to the CDP1802 microprocessor in a 4096-byte RAM system.

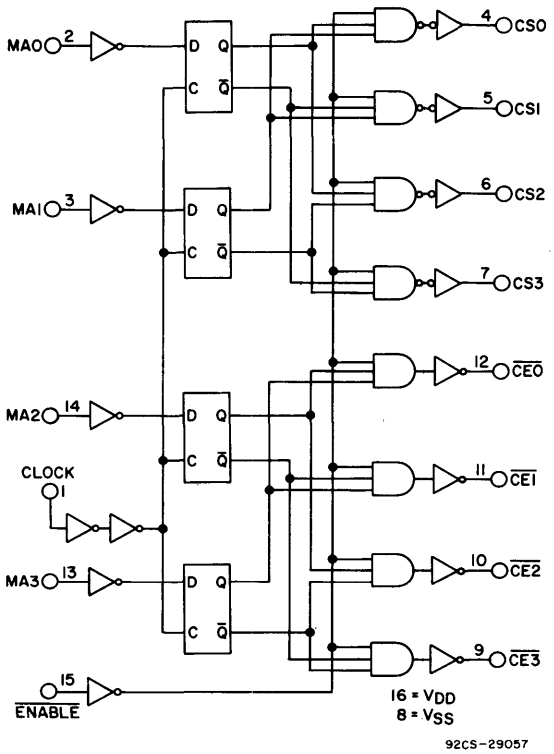


Fig. 211 – Functional diagram for the CDP1858, 4-bit latch with decode.

XII. Circuits and Applications

The circuits in this section illustrate some of the applications that can be implemented using the RCA CD4000 series of COS/MOS integrated circuits. The selection has been made to show a wide variety of circuit ideas and to indicate the ease with which different logic operations and functions can be realized.

Logic functional diagrams and operating waveforms are shown for a broad range of circuits in which the low quiescent dissipation, well-defined logic levels, high noise immunity, and other features of the CD4000-series devices result in significant advantages. Brief summations are given of the over-all logic function of the various circuits. Detailed information on the operation of basic circuit elements, such as gates, inverters, flip-flops, counters, and registers, that may be included in the various circuit arrangements is given in earlier sections of this Manual.

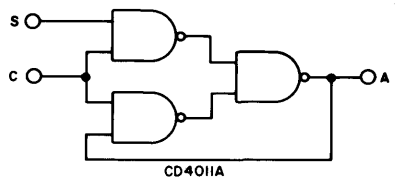
In many of these circuits, where an A-series type is indicated, the type may be replaced by a B-series type if the higher supply-voltage rating of the B-series is required by the specific application. Similarly, where a B-series is specified, it may be replaced by an A-series type if the lower operating voltage of the A-series is adequate for the application. Check the databook **RCA COS/MOS Integrated Circuits SSD-250** for information on A- and B-series types.

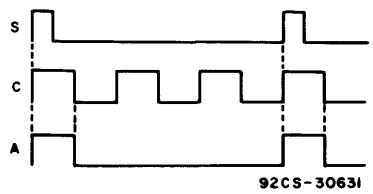
List of Circuits

List of Circuits
(continued)

Circuit No. 1 - PULSE STRETCHER

This circuit illustrates the use of the CD4011 quad 2-input NAND gate as a pulse stretcher. The signals at terminals S and C are synchronized. The pulse duration of the signal at terminal S, however, is much shorter than that of the signal at terminal C. The feedback loop from the output (terminal A) stretches out the pulse at S to equal the length of the pulse at C. Any time the pulse at S is not present, the output is zero. The repetition rate of C can, therefore, be any convenient multiple of the basic S rate. The output signal has a pulse duration equal to that of the signal applied to terminal C and the same repetition as the signal applied to terminal S. The circuit waveforms shown indicate the relationship between output and input pulses when the repetition rate of the signal at C is three times that of the signal at S.

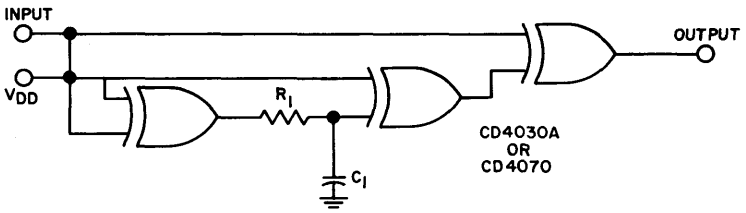


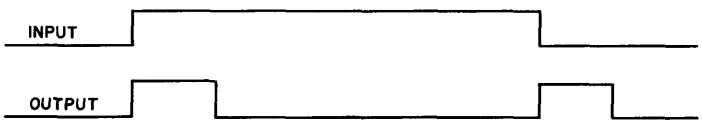


Circuit No. 2 - TRANSITION DETECTOR/FREQUENCY DOUBLER

This circuit shows an arrangement for use of the CD4030 or CD4070 quad exclusive-OR gate to detect logic-level changes. A transition from low to high or from high to low produces a pulse at the output terminal of the gate. The duration of the output pulse can be varied by a change in the time constant of the resistance-capacitance network formed by R_1 and C_1. The section of this Manual on Astable and Monostable

Multivibrators explains how the desired values of resistor R_1 and capacitor C_1 are determined. Because two output pulses are produced for each input pulse, this circuit is also useful as a frequency doubler.



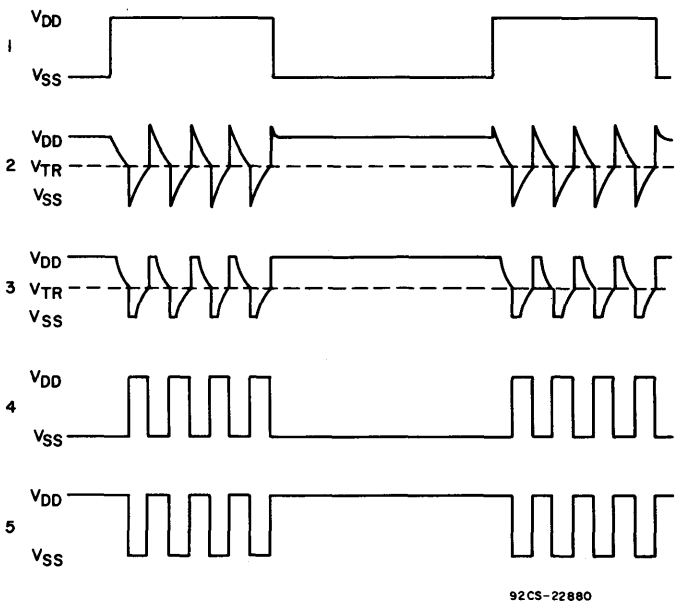


92CS-30632

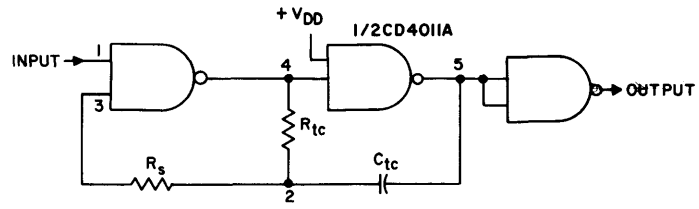
Circuit No. 3 - PULSE MODULATOR

Pulse modulation may be accomplished by use of this circuit which utilizes a CD4011 quad 2-input NAND gate. The oscillator is gated ON or OFF by the signal input at Pin 1 of the NAND gate.

Note that the third (buffer) stage has the two inputs to its NAND gate tied together, while the second stage has one input tied to $+V_{DD}$. Both stages act as inverters. It is important, however, that the second stage, which is an active part of the oscillator circuit, have the same gain and transfer characteristics as the first oscillator stage, which uses only one p and n pair for amplification. The waveforms at five points in the circuit are shown.

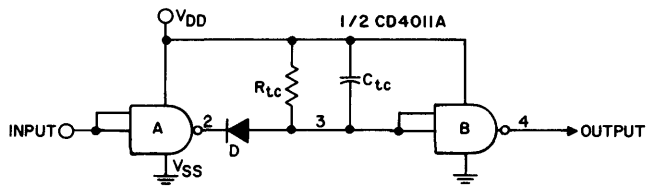


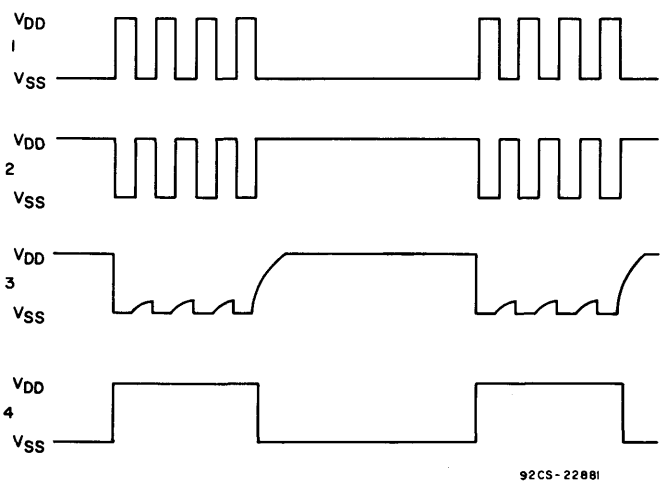
92CS-22880



Circuit No. 4 - DEMODULATOR

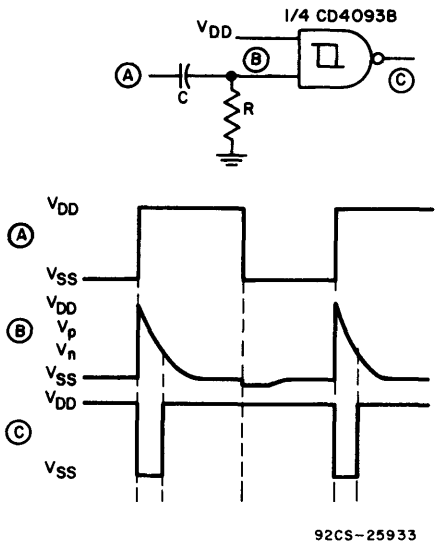
Demodulation or envelope detection of pulse-modulated waves is performed by this circuit which utilizes the CD4007 dual complementary pair plus inverter. The carrier burst input is inverted (byInverter A), and its first negative transition at point 2 turns on the diode (D) to provide a charging path for capacitor C_{tc} through the n-channel resistance to ground. On the positive transition of the signal (at point 2), the diode is cut off and C_{tc} discharges through R_{tc}. The discharge time constant (R_{tc} C_{tc}) is much greater than the time of the burst duration. Point 3, therefore, never reaches the switch point of inverter B until the burst has ended. The waveforms at four points in the circuit are shown.



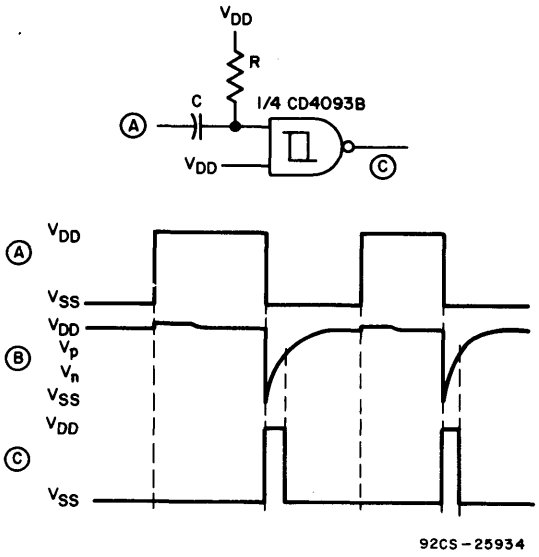


Circuit No. 5 - EDGE DETECTORS

These circuits using the Schmitt trigger CD4093 are for detecting either positive-going or negative-going edges. Circuit (a) provides a short negative-going output pulse for every positive-going edge at the input. The input waveform is coupled to the input by capacitor C and the pulse length depends on the values of R and C. For a negative-going edge detector, circuit (b) is suggested.



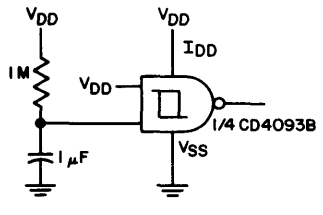
(a)



(b)

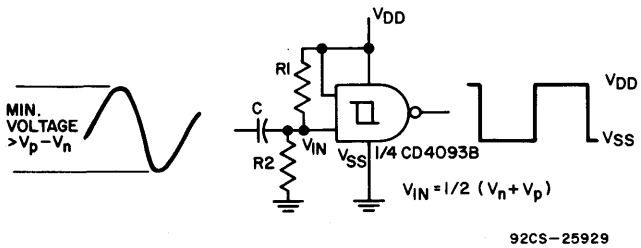
Circuit No. 6 - POWER-ON RESET

A reset pulse is often required at power-on in a digital logic system. This type of reset pulse is provided by this circuit. Because of the high input impedance of the Schmitt trigger, long reset pulse times may be achieved without the excess dissipation that would result with gates other than Schmitt triggers when both output devices are on simultaneously.



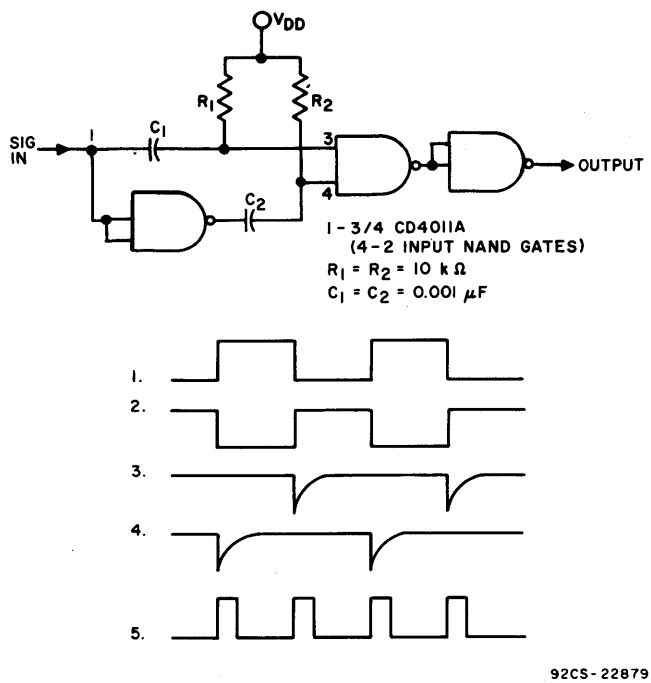
Circuit No. 7 - SINE-WAVE TO SQUARE-WAVE CONVERTER

This circuit shows a typical application of the Schmitt trigger, the sine-wave to square-wave converter. The sine input is ac coupled by capacitor C; resistors R1 and R2 bias the input midway between Vn and Vp, the input threshold voltages, to provide a square wave at the output.



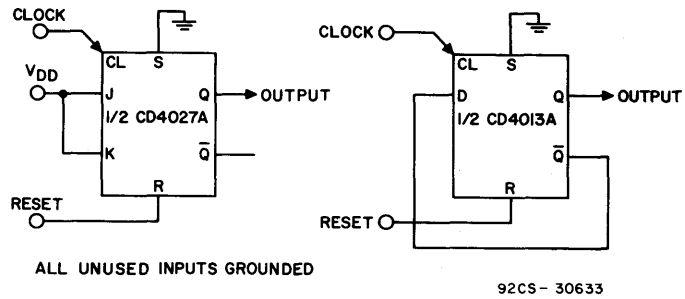
Circuit No. 8 - FREQUENCY DOUBLER

This circuit shows a frequency doubler using a quad 2-input NAND gate CD4011. A 2^N multiplier can be realized by cascading this circuit with N-1 other identical circuits. The leading edge of the input signal is differentiated by R1 and C1, applied to the input terminal 1 of the NAND gate, and produces a pulse at the output. The trailing edge of the input pulse, after having been inverted, is differentiated, applied to input terminal 2 of the NAND gate, and produces the second output pulse from the NAND gate. The waveforms at five points in the circuit are shown.



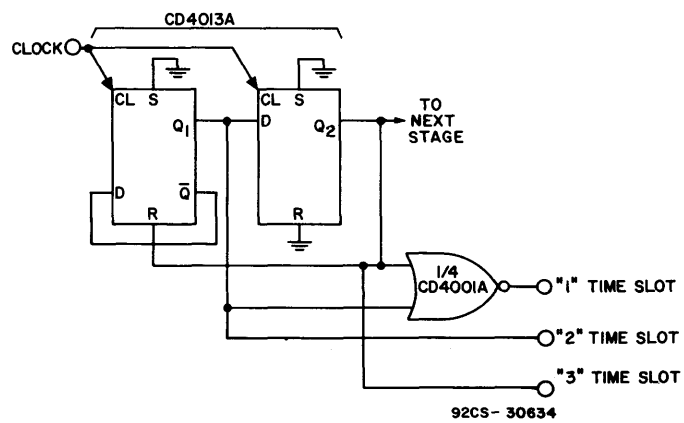
Circuit No. 9 - DIVIDE-BY-2 COUNTERS

These circuits illustrate the use of one-half a CD4027 dual J-K master-slave flip-flop and one-half a CD4013A dual "D" type flip-flop to form two simple divide-by-2 counters. The CD4013A counter is made to toggle by returning the $\overline{Q}$ output to the D input.



Circuit No. 10 - DIVIDE-BY-3 SYNCHRONOUS COUNTER WITH DECODED OUTPUTS

In this circuit, both sections of a CD4013 dual "D" type flip-flop are interconnected with one gate unit of a CD4001 quad two-input NOR gate to form a divide-by-3 synchronous counter with three decoded outputs.

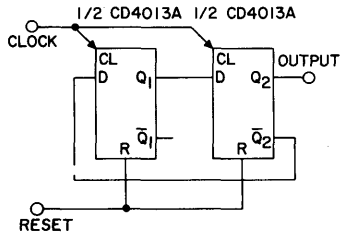


SEQUENCE

Q_2	Q_1	TIME SLOT
0	0	"1"
0	1	"2"
1	0	"3"
0	0	"1"

Circuit No. 11 - DIVIDE-BY-4 SYNCHRONOUS COUNTER

This circuit illustrates the use of both sections of a CD4013A dual "D" type flip-flop in a divide-by-4 synchronous counter. A high level on the reset line forces the counter into the "0" state.



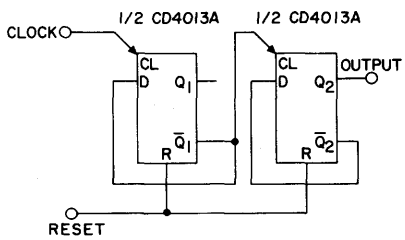
SEQUENCE (JOHNSON) Q_2	Q_1	STATE
0	0	0
0	1	1
1	1	2
1	0	3
0	0	0

ALL UNUSED SETS GROUNDED

92CS-30635

Circuit No. 12 - DIVIDE-BY-4 RIPPLE COUNTER

In this circuit, the two sections of a CD4013A dual "D" type flip-flop are interconnected to form a divide-by-4 ripple counter. A comparison of the truth table for this circuit with that for the synchronous counter (Circuit No. 11) shows the variation in the logic sequences for ripple and synchronous counters that provide the same count division. As with the synchronous type, a high level on the reset line forces the divide-by-4 ripple counter into the "0" state.

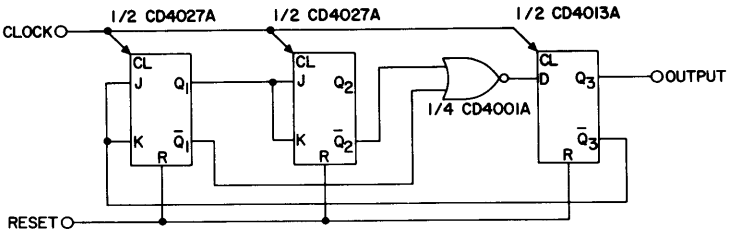


SEQUENCE Q_2	Q_1	STATE
0	0	0
0	1	1
1	0	2
1	1	3
0	0	0

92CS-30636

Circuit No. 13 - DIVIDE-BY-5 SYNCHRONOUS COUNTER

In this circuit, both sections of a CD4027A dual J-K flip-flop, a single gate unit of the CD4001A quad two-input NOR gate, and one section of a CD4013A dual "D" type flip-flop are interconnected to form a divide-by-5 synchronous counter. A high level on the reset line forces the counter into the "0"state.



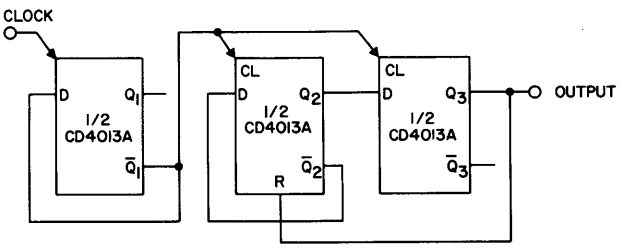
ALL UNUSED SETS GROUNDED
ALL UNUSED GATE INPUTS GROUNDED

SEQUENCE			
Q_3	Q_2	Q_1	STATE
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
0	0	0	0

92CS-30637

Circuit No. 14 - DIVIDE-BY-6 RIPPLE COUNTER

This circuit shows that a single flip-flop section of a CD4013A dual "D" type flip-flop can be added in cascade with the CD4013A divide-by-4 ripple counter to provide a divide-by-6 ripple counter.



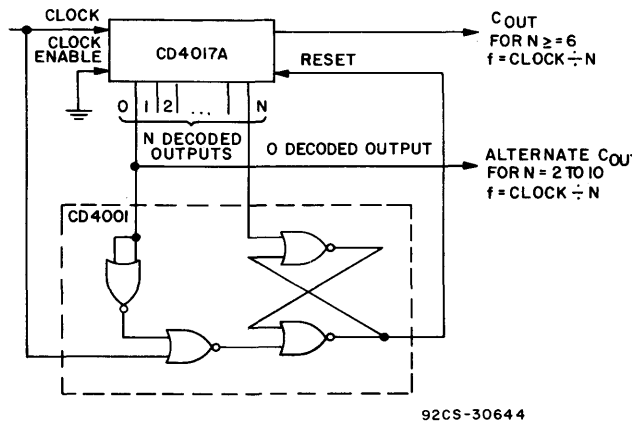
ALL UNUSED SETS AND RESETS GROUNDED

92CS-30638

SEQUENCE			
Q_3	Q_2	Q_1	STATE
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
0	0	0	0

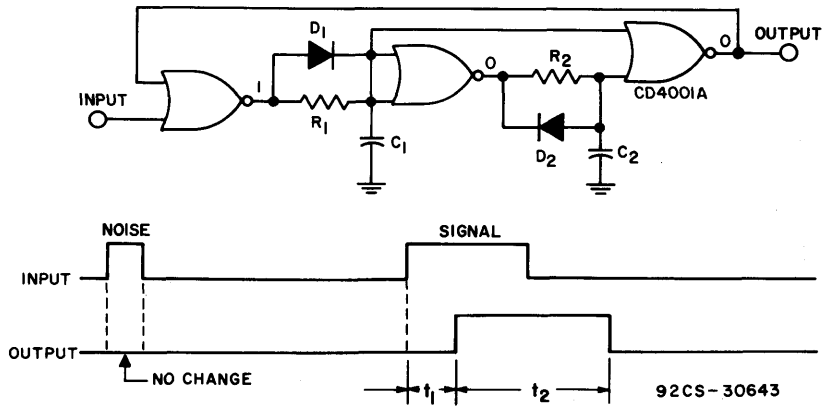
Circuit No. 15 - DIVIDE-BY-N COUNTER WITH N DECODED OUTPUTS

This circuit illustrates the use of a CD4017A decade counter/divider and a CD4001A dual 2-input NOR gate in a divide-by-N counter that provides N decoded outputs. When the Nth decoded output is reached (Nth clock pulse), the S-R flip-flop (constructed from two NOR gates of the CD4001) generates a reset pulse which clears the CD4017A to its zero count. If the Nth decoded output is greater than or equal to 6, the clock-output (C_{OUT}) line goes high to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of a low clock and a low decoded "0" output resets the S-R flip-flop to enable the CD4017A. If the Nth decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used to clock the next counter. In this case, the "0" decoded output may be used to perform this clocking function.



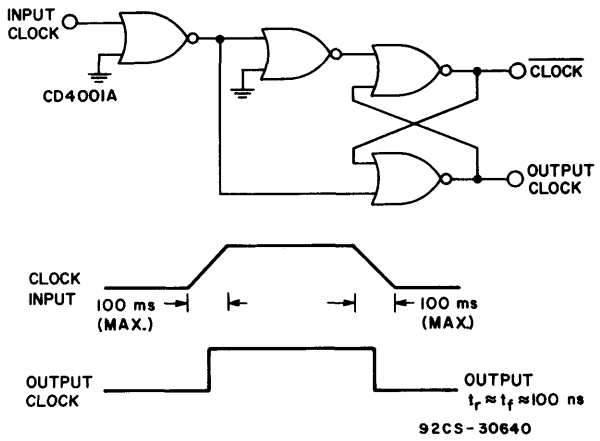
Circuit No. 16 - NOISE DISCRIMINATOR USING NOR GATES

In this circuit, the CD4001A quad two-input NOR gate is used in a noise-discriminator application. The circuit discriminates between noise pulses that last less than a specific duration t_1 and pulses that have a duration greater than t_1. An input pulse that has a duration greater than t_1 produces an output of pulse duration t_2. The time t_1 is determined by the time constant of resistor R1 and capacitor C1 (i.e., $t_1 = R_1C_1$). The time t_2 is determined by the time constant of resistor R_2 and capacitor C_2 (i.e., $t_2 = R_2C_2$). Diodes D_1 and D_2 allow fast recovery.



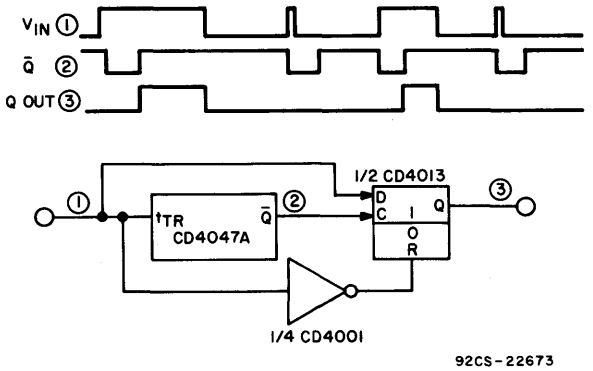
Circuit No. 17 - CLOCK EDGE SHAPING CIRCUIT

This circuit illustrates how a CD4001A quad two-input NOR gate may be used to reshape the rise and fall times of clock pulses that have slow transition times. Shorter transition times of the output clock pulse result from the regeneration action of the output flip-flop. Complementary clock outputs are also available. With this circuit, an input clock pulse that has rise and fall times of 100 milliseconds can be reshaped so that the transition times are reduced to 100 nanoseconds.



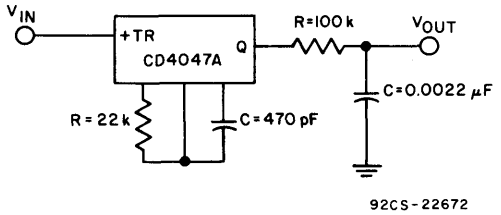
Circuit No. 18 - NOISE DISCRIMINATOR USING MULTIVIBRATOR

This circuit illustrates an application of a CD4047A low-power monostable/astable multivibrator in a noise discriminator. By adjusting the external time constant, a pulse width narrower than that determined by the time constant is rejected by the circuit. The output pulse follows the desired input, but the leading edge is delayed by the selected time constant.



Circuit No. 19 - FREQUENCY DISCRIMINATOR

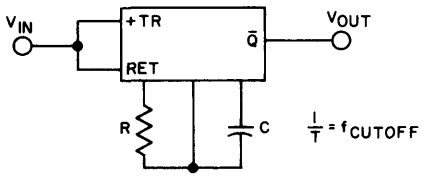
This circuit illustrates the rise of the CD4047A low power monostable/stable multivibrator as a frequency-to-voltage converter. A waveform of varying frequency is applied to the +TR (trigger) input. The one-shot produces a pulse of constant width for each positive transition on the input. The resultant pulse train is integrated to produce a waveform having an amplitude proportional to the input frequency.



92CS-22672

Circuit No. 20 - LOW-PASS FILTER

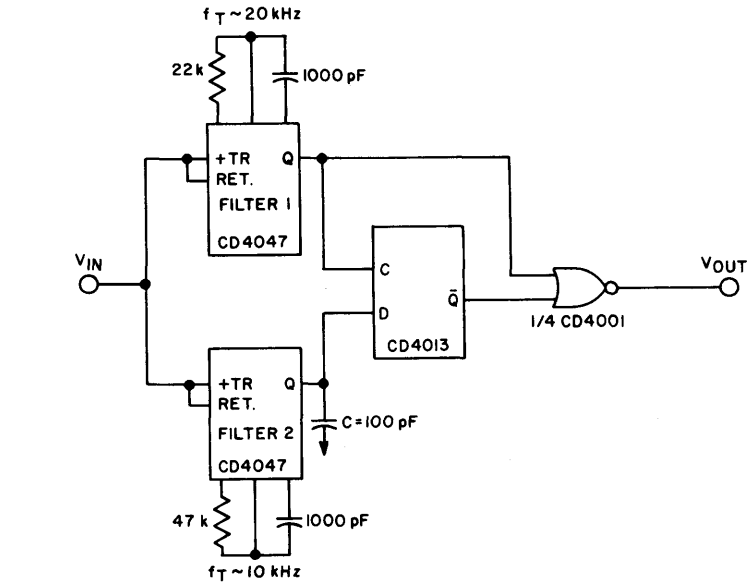
This simple circuit uses the CD4047A low-power monostable/astable multivibrator as a low-pass filter. The time constant chosen for the multivibrator determines the upper cutoff frequency for the filter. The circuit essentially compares the input frequency with its own reference. It then produces an output that follows the input for frequencies less than the cut off frequency and a low output for frequencies greater than the cut off frequency.

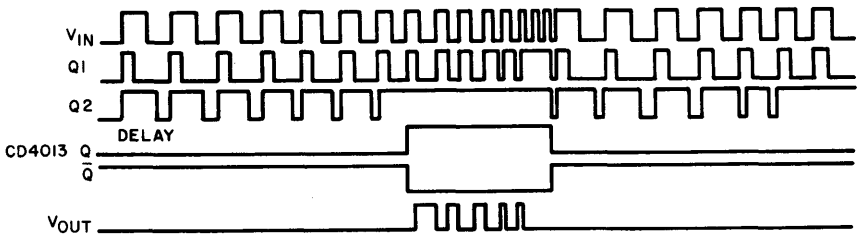


92CS-22671

Circuit No. 21 - BANDPASS FILTER

Two CD4047A low-pass filters can be used to construct a bandpass filter, as illustrated in this circuit. The pass band is determined by the time constants of the two filters. If the output of filter No. 2 is delayed by capacitor C_1, the CD4013A flip-flop will clock high only when the cutoff frequency of filter No. 2 has been exceeded; this point is illustrated in the timing waveforms. The $\overline{Q}$ output of the CD4013A is gated with the output of filter No. 1 to produce the desired output.





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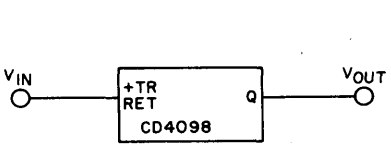
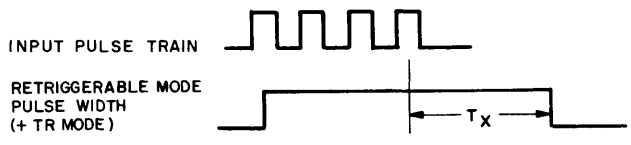
Circuit No. 22 - ENVELOPE DETECTOR

The CD4098 dual monostable multivibrator can be used as an envelope detector by employing it in the retrigger mode, as shown in this circuit. A retriggerable one-shot multivibrator has a time period T_X referenced from the application of the last input pulse. The time constant is selected so that the circuit registers at the frequency of the input pulse burst. A dc level appears at the output for the duration of the input pulse train.

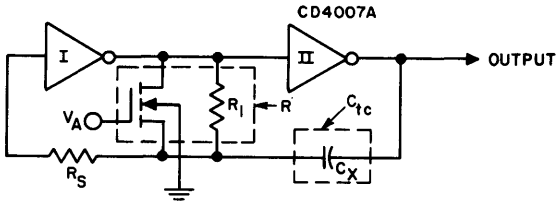




92CS-30676

Circuit No. 23 - VOLTAGE-CONTROLLED OSCILLATOR

This circuit is similar to the RC oscillator shown in Fig. 94, except that the time-constant resistor R_{tc} is replaced by two components in parallel, R1 and an n-channel device. Both inverters and the n-channel device are available in a single CD4007 package. As the potential at V_A varies from V_{SS} to V_{DD}, the impedance of the n-channel device varies from 10^9 ohms (OFF) to 1 kilohm (ON). Thus, R_{tc} will vary from 10 kilohms to 1 kilohm. C_{tc}, which controls the oscillator center frequency, is varied by adjustment of capacitor C_x. The tabulation shows the variation of the output waveform period as a function of V_{DD} and V_A.



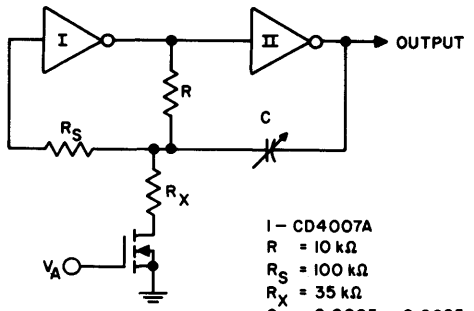
TYPICAL VALUES:
R_1 = 10 kΩ C_X = 0.001 – 0.004 μF
R_S = 100 kΩ $0 \le V_A \le V_{DD}$

92CS-22878RI

V_A (V)	Period (μs)		
	V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 15 V
C	120	54	48
5	115	45	41
10	–	32	30
15	–	–	24

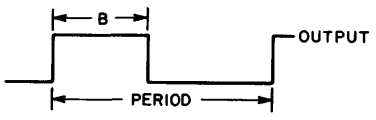
Circuit No. 24 - VOLTAGE-CONTROLLED PULSE-WIDTH CIRCUIT

This circuit is a further modification of Fig. 94. In this circuit the pulse width is modulated (by varying V_A) only if R_x is sufficiently high. As an example, if C = 0.0022 microfarads, then $R_x \simeq 35$ kilohms. Lower values of R_x cause the frequency to be affected. If R_x is lower than 10 kilohms, there is a value of V_A that will cause the oscillator to cut off. The tabulation lists values of pulse width (B) for various values of V_A and V_{DD}. The output waveform for the circuit described is also shown.



I – CD4007A
R = 10 kΩ
R_S = 100 kΩ
R_X = 35 kΩ
C = 0.0005 – 0.0025 μF

(a)



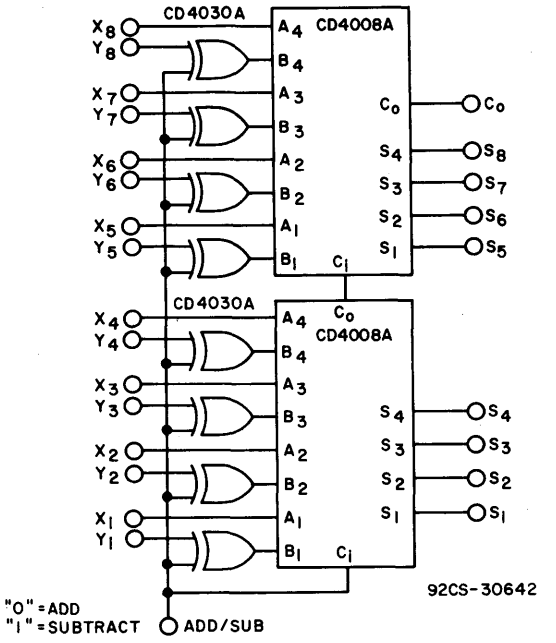
(b)

92CS-22882RI

V_A (V)	Pulse Width (B) μs		
	V_{DD} = 5 V Period -41.5	V_{DD} = 10 V Period-35	V_{DD} = 15 V Period-33
0	23	19.3	17
5	20	17.7	16.2
10	–	16.2	15.5
15	–	–	14.3
C_{tc} = 0.0016 μF			

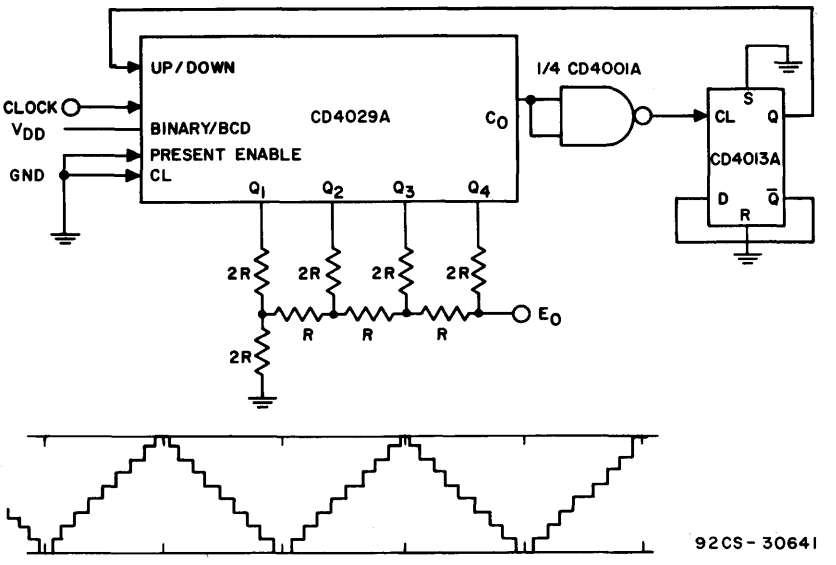
Circuit No. 25 - TWO'S COMPLEMENT ADDER-SUBTRACTER

This circuit illustrates the use of two CD4008A four-bit full adders together with two CD4030A quad exclusive-OR gates to perform two's-complement addition and subtraction. With a "0" on the Add/Sub line, the number $Y_1Y_2...Y_8$ is not inverted, and the number $X_1X_2...X_8$ is added to the numbers $Y_1Y_2...Y_8$. When "1" is on the Add/Sub line, the number $Y_1Y_2...Y_8$ is inverted, and the CARRY IN is made a "1" to make the two's complement of the number $Y_1Y_2...Y_8$. The number $Y_1Y_2...Y_8$ is added to the number $X_1X_2...X_8$ to complete the subtraction.



Circuit No. 26 - FUNCTION GENERATOR

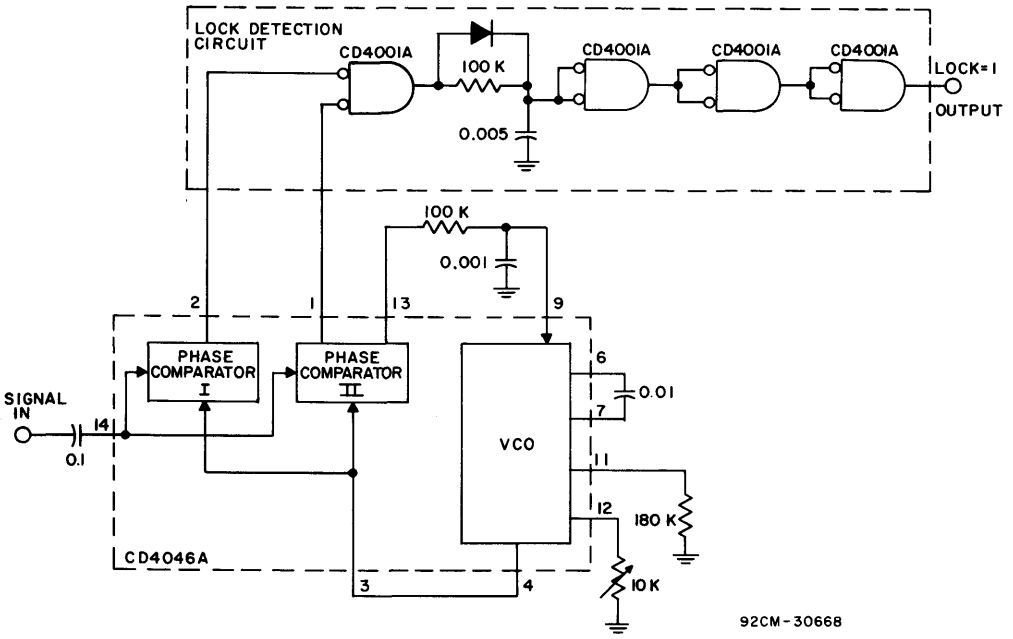
In this circuit, a CD4029A presettable up/down BCD counter is interconnected with a CD4013A "D"-type flip-flop to generate the "stair-case" waveform shown. As the CD4029A is clocked up to its final count, the clock output C_0 goes from a high to a low. This output is inverted by the CD4001A and used to toggle the D flip-flop. This toggling action changes the mode of counting from up to down. When the count gets to 0000, C_0 again goes from high to low, and the mode control goes from down to up.



Circuit No. 27 - PHASE-LOCKED-LOOP LOCK-DETECTION CIRCUIT

In some applications that utilize a phase-locked loop (PLL), it is sometimes desirable to have an output indication of when the PLL is in lock. One of the simplest forms of lock-condition indicator is a binary signal. For example, a "1" or a "0" output from a lock-detection circuit would correspond to a locked or unlocked condition, respectively. This signal could, in turn, activate circuitry utilizing a locked PLL signal. This detection could also be used in frequency-shift-keyed data transmissions in which digital information is transmitted by switching the input frequency between either of two discrete input frequencies, one corresponding to a digital "1" and the other to a digital "0".

In this lock-detection circuit, the signal input is switched between two discrete frequencies: 20 kHz and 10 kHz. The PLL system uses phase-comparator II. Because the bandwidth of the voltage-controlled oscillator is set up for a minimum frequency of 9.5 kHz and a maximum frequency of 10.5 kHz, the PLL locks on the 10-kHz signals and unlocks on the 20-kHz signals. When the PLL is in lock, the output of phase-comparator I is low except for some very short pulses that result from the inherent phase difference between the signal and comparator inputs. The phase-pulses output (terminal 1) is high except for some very small pulses resulting from the same phase difference. This low condition of phase comparator I is detected by the lock-detection circuit.

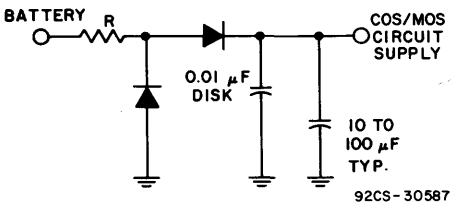


Circuit No. 28 - TRANSIENT-PROTECTION CIRCUIT FOR AUTOMOBILE DIGITAL LOGIC SYSTEMS

An adequate transient-protection circuit is an essential part of any automobile digital logic system. Although automobile manufacturers disagree on the maximum amplitude and decay of transient voltage, the transient extremes often used are +120 volts and -90 volts, each decaying exponentially with a maximum time constant of 400 milliseconds. Because B-series COS/MOS circuits are rated for a maximum recommended supply of 18 volts (and A-series at a lower value), a protection circuit must be

included between the automobile battery and the COS/MOS logic.

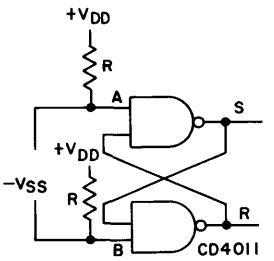
This figure shows a transient-voltage protection circuit that is frequently used. The zener diode regulates the voltage supply for the COS/MOS circuits, and the capacitor and series diode prevent voltage loss during negative transients. A small diode capacitor, shown in parallel with the output, gives rf protection during transients. For minimum zener current during transients, the maximum value of R should be based on the minimum circuit operating voltage and the peak current drawn by the logic circuit at the minimum battery voltage. The minimum zener breakdown voltage is then determined by subtraction of the product of the minimum current drain at the normal battery voltage and the value of R just chosen from the battery voltage. A zener breakdown greater than this voltage assures that no unnecessary current will be drawn by the zener during normal automobile operation.



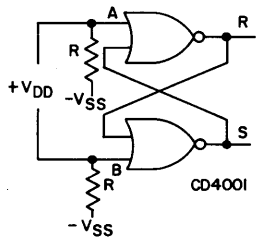
Another important characteristic of the zener selected is its dynamic impedance. During a current surge, the voltage across the zener must not rise to a damaging level. A value of 20 volts is safe for COS/MOS B-series circuits.

Circuit No. 29 - SWITCH DEBOUNCING CIRCUITS

Contact bounce, the uncertainty that occurs as a mechanical switch closes, can cause troublesome transitions in logic circuits. Such uncertainties are normally overcome by providing a delay at the input sufficient to assure that the signal recognized is a true one. The amount of delay needed varies with the type of switch used. The "bounce" can be as long as several hundred milliseconds. Three typical debounce circuits are given.

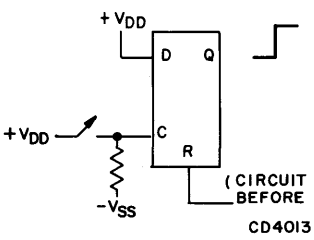


SWITCH			
A	B	S	R
0	0	1	1
0	1	1	0
1	0	0	1
1	1	NC*	



SWITCH			
A	B	S	R
0	0	NC*	
0	1	0	1
1	0	1	0
1	1	0	0

*NC = NO CHANGE

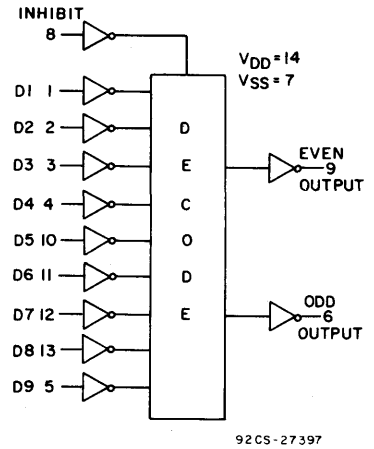


RESET	CLOCK	Q
1	–	0
0	–	0
0	1	1
0	–	1

Circuit No. 30 - NINE-BIT PARITY GENERATOR/CHECKER

The RCA-CD40101 is a nine-bit (eight data bits plus one parity bit) parity generator/checker. It may be used to detect errors in data transmission or data retrieval. Odd and even outputs from the device facilitate odd or even parity generation and checking. When the CD40101 is used as a parity generator, a parity bit is supplied along with the data to generate an even or odd parity output. When it is used as a parity checker, the received data bits and parity bits are compared for correct parity. The even or odd outputs are used to indicate an error in the received data.

Word length is expandable by cascading. The CD40101 is also provided with an inhibit control. If the inhibit control is set at logical "1", the even and odd outputs go to a logical "0".



Truth Table

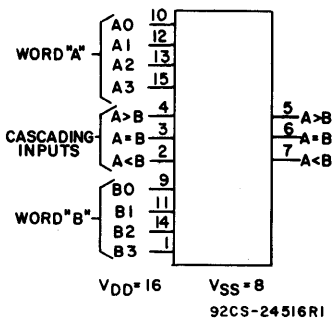
Inputs		Outputs	
D1-D9	Inhibit	Even	Odd
Σ 1's=Even	0	1	0
Σ 1's=Odd	0	0	1
X	1	0	0

X = Don't Care
Logic 1 = High
Logic 0 = Low

Circuit No. 31 - FOUR-BIT MAGNITUDE COMPARATOR

The RCA-CD4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063 has eight comparing inputs (A3, B3 through A0, B0), three outputs (A<B, A=B, A>B), and three cascading inputs that permit systems designers to expand the comparator function.



XIII. Custom LSI Design

In the early chapters of this Manual, information was given about the operation and characteristics of COS/MOS devices to assist the designer in using use packaged small-scale and medium-scale integrated COS/MOS devices effectively. Later chapters gave detailed information on the logical functions that many of RCA's commercial COS/MOS units provide. At some point after the successful engineering of a digital logic design (which may incorporate a number of SSI and MSI circuits), the question often arises as to the feasibility of integrating the design into a single LSI custom chip. This chapter will describe the various factors that should be considered in making this decision and the several approaches that can be taken in integrating a design. First, however, it would be appropriate to provide some background information on COS/MOS processing and more detailed information on discrete device characteristics than was necessary for "building-block" engineering. (This next section may be considered a continuation of Chapter I COS/MOS Integrated Circuit Fundamentals).

MOS DESIGN PARAMETERS

As stated in Chapter I, an enhancement-mode MOS transistor is basically a voltage-controlled device that exhibits a capacitive input and conducts initially when the gate-to-source voltage is equal to the threshold voltage.

Threshold Voltage

The threshold voltage V_{TH} for a p-channel enhancement-type unit is given by

$$V_{TH} = V_{TO} - K_B[(V_{BS} + \psi^{1/2}) - (\psi)^{1/2}] \quad (13\text{-}1)$$

where K_B is a function of the carrier concentration of the substrate, V_{BS} is the substrate-to-source voltage, ψ is the surface potential, and V_{TO} is the negative threshold value for $V_{BS} = 0$. The change in V_{TH} as a function of V_{BS} is plotted for several n-type substrate resistivities in Fig. 212. The

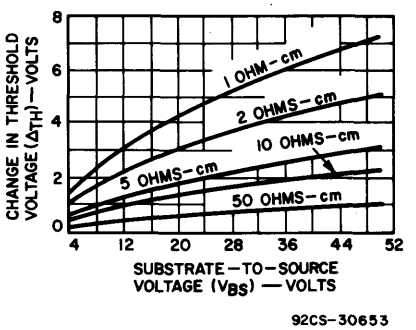


Fig. 212 – Change in threshold voltage as a function of V_{BS} for several n-type substrate resistivities.

boundary between the regions in which Eqs. (13-1) and (13-2) apply corresponds to the condition $V_{DS} = V_{GS} - V_{TH}$, and is shown as the dashed line in Fig. 213. The equations given here are ideal in that the finite drain resistance in the saturation region ($0 \leqslant V_{GS} - |V_{TH}| \leqslant V_{DS}$), the series parasitic resistance, the variation of channel mobility with gate-to-source voltage, and the drain-to-source leakage current are all neglected.

Threshold voltage can also be defined as follows:

$$V_{TH} = \frac{t_{ox}S}{\epsilon} + \psi_{MS} + 2\psi_f \qquad (13\text{-}2)$$

where t_{ox} is the oxide thickness, ϵ is the electrical permittivity of the oxide, ψ_{MS} is the difference between metal and semiconductor work functions, ψ_f is the difference in Fermi potential between the inverted surface and the bulk of semiconductor, and

$$S = \psi_{SS} + \psi_B$$

where ψ_{SS} is the fixed surface-state charge, ψ_B is the bulk charge of silicon, and S equals the sum of these charges.

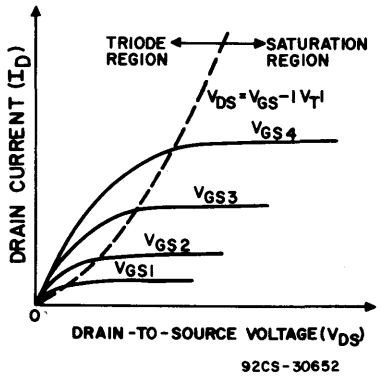


Fig. 213 – Drain current as a function of drain-to-source voltage in a p-channel enhancement-type MOS transistor.

Current-Voltage Relationships

Fig. 213 shows the theoretical curve of drain-to-source current I_D as a function of drain-to-source voltage V_{DS} and gate-to-source voltage V_{GS} for a p-channel enhancement-type MOS transistor. The "ideal" equations for these characteristics in the various operating regions are as follows:

1. In the triode region, i.e.,

$$0 \leqslant V_{DS} \leqslant (V_{GS} - |V_{TH}|)$$

drain-to-source current is defined by the following relationship:

$$I_D = \frac{\mu\epsilon}{2t_{ox}} \left\{ \frac{W}{L} \left[2(V_{GS} - |V_{TH}|)V_{DS} - V_{DS}^2 \right] \right\} \qquad (13\text{-}3)$$

2. In the saturation region, i.e.,

$$0 \leqslant (V_{GS} - |V_{TH}|) \leqslant V_{DS}$$

the drain-to-source current is given by

$$I_D = \frac{\mu\epsilon}{2t_{ox}} \left[\frac{W}{L} (V_{GS} - V_{TH})^2 \right] \qquad (13\text{-}4)$$

where μ is the effective surface mobility of the carriers in the channel, and W and L are channel dimensions.

3. When the gate-to-source voltage is less than the threshold voltage, i.e., $V_{GS} \leqslant |V_{TH}|$, the drain-to-source current becomes

$$I_D = 0$$

These equations can be simplified by introducing a factor which combines those characteristics fixed by the manufacturing process in one component and those determined by device geometry in another component:

$$K = \frac{\mu\epsilon W}{2t_{ox}L} = \left(\frac{\mu\epsilon}{2t_{ox}}\right)\frac{W}{L} = K'\frac{W}{L}$$

where

$$K' = \frac{\mu\epsilon}{2t_{ox}}$$

(all characteristics determined by processing) and W/L is the device geometry (channel length "L" is the spacing between the source and drain; channel width "W" is the dimension of the drain edge along the channel).

The range of K' for RCA manufacturing processes is given below for n- and p-type devices.

Range of K'	Min.	Typ.	Max.	Units
K'_n	6	8	10	$\mu A/V^2$
K'_p	2	3	4	$\mu A/V^2$

By use of the K-factor simplification, Eq. (13-3) for the triode region becomes

$$I_D = 2K\left[V_{DS}(V_{GS} - V_{TH}) - \frac{V_{DS}^2}{2}\right] \quad (13\text{-}5)$$

and Eq. (13-4) for the saturation region becomes

$$I_D = K(V_{GS} - V_{TH})^2 \quad (13\text{-}6)$$

Transconductance

The transconductance g_m is given by the following relation.

$$g_m = \left.\frac{\partial I_{SD}}{\partial V_{GS}}\right|_{V_{DS} = \text{constant}} \quad (13\text{-}7)$$

or

$$g_m = \frac{\mu \epsilon W}{t_{ox} L}(V_{GS} - |V_{TH}|) \quad (13\text{-}8)$$

By substitution and use of the k factor:

$$g_m = 2K(V_{GS} - |V_{TH}|) \quad (13\text{-}9)$$

Channel Dimensions

Although the K' factor is set by the manufacturing process and cannot be varied, in the layout design of COS/MOS integrated circuits the length and width of the channel can be increased or decreased, within tolerance specifications, to meet the requirements of particular applications.

For high-transconductance (low-impedance) devices, the channel length is decreased to its minimum value, and the channel width is made as large as required to provide the desired current. Figs. 214 and 215 show the drain characteristics and K' values for the CD4007A. Fig. 216 shows the effect of channel width on the drain current of both p and n MOS transistors.

The minimum value of the channel length (source-to-drain spacing), as established by

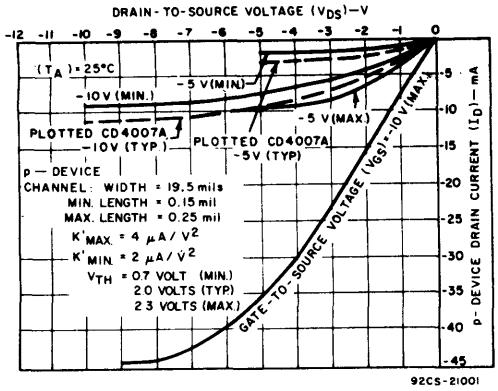


Fig. 214 — Maximum and minimum p-device drain current characteristics for type CD4007A.

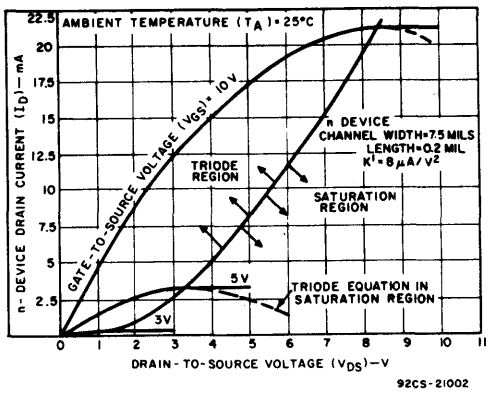


Fig. 215(a) — Typical n-device drain current characteristics for type CD4007A.

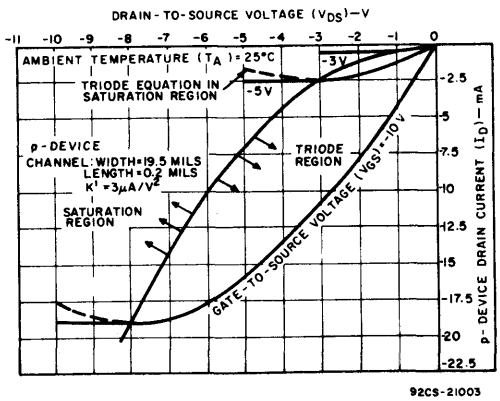


Fig. 215(b) — Typical p-device drain current characteristics for type CD4007A.

processing and voltage punch through considerations, is 0.3 mil. The channel width in typical COS/MOS products ranges from approximately 0.4 mil to 200 mils.

For low-transconductance (high-impedance) devices, the channel width is

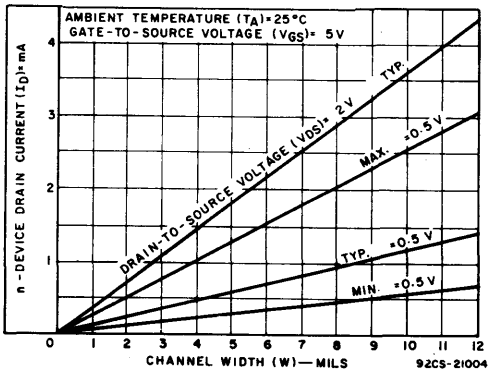


Fig. 216(a) — Drain current as a function of channel width for an n device at a gate-to-source voltage of 5 volts.

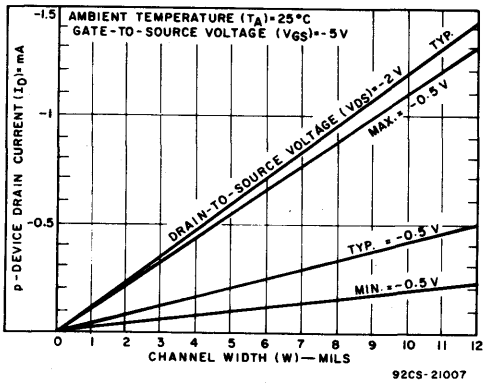


Fig. 216(b) — Drain current as a function of channel width for a p device at a gate-to-source voltage of −5 volts.

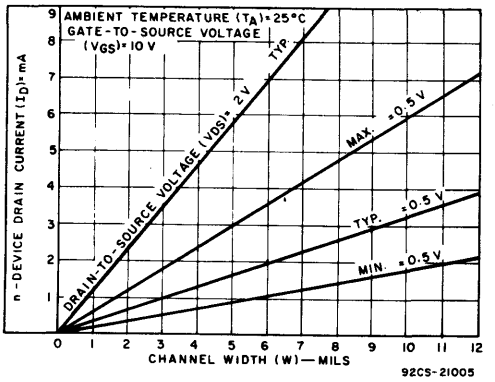


Fig. 216(c) — Drain current as a function of channel width for an n device at a gate-to-source voltage of 10 volts.

decreased to its minimum value, and the channel length is made as long as necessary to provide the required impedance. The minimum channel width, determined by processing and photoengraving con-

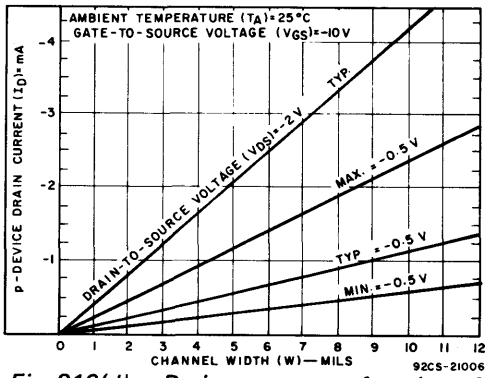


Fig. 216(d) — Drain current as a function of channel width for a p device at a gate-to-source voltage of −10 volts.

siderations, is 0.4 mil. Channel length can be varied from a minimum value of 0.3 mil up to several mils. Channel width also affects the source-to-drain transition time as a function of load capacitance because of the increased current drive. Figs. 217(a) and (b) show the relationship of these parameters for both n-channel and p-channel MOS transistors.

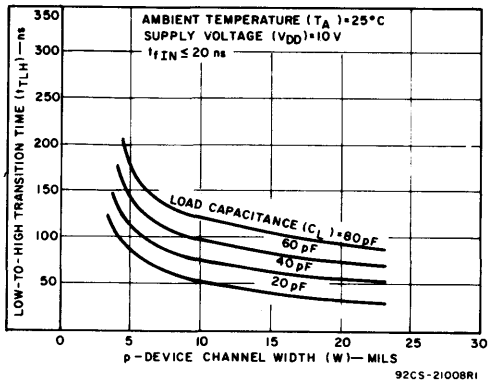


Fig. 217(a) — Transition time as a function of channel width and load capacitance for p-channel devices.

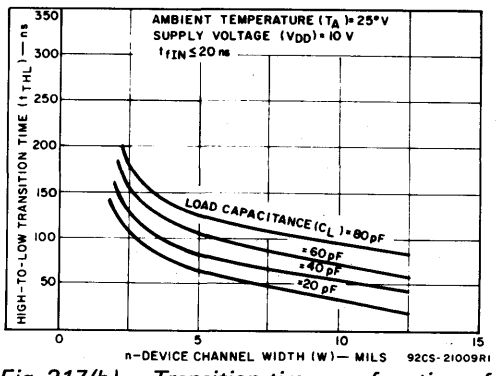


Fig. 217(b) — Transition time as a function of channel width and load capacitance for n-channel devices.

Input Capacitance

For switching purposes, it is important to know the input capacitance. As shown in Fig. 218, input capacitance is made up of four elements:

A. The package and pin; bond wire; bond pad
B. Input protective circuit
C Metallized conductor leading to gate
D. Gate capacitance

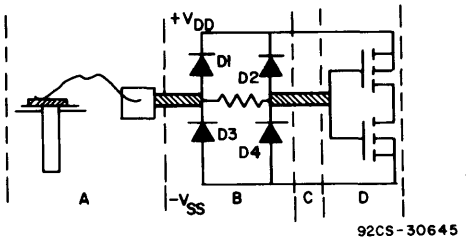


Fig. 218 – Input capacitance elements.

A. The bond pad is a 0.4-mil square metallized on thick oxide over the N+ region. Its contribution (C_{bp}) is 0.004 picofarad. The bond wire, package pad, and pin (C_p) add just under 1 picofarad.

B. The protective circuit consists of a diffused resistor (which also forms distributed diodes D_1 and D_2) and diodes D_3 and D_4. This capacitance C_r is 0.56 picofarad. Diodes D_3 and D_4, which are forward biased for fastest response, contribute about 1 picofarad capacitance each (C_D = 2 picofarads).

C. The length of the metallized conductors (including bond pad to protective circuit and protective circuit to gate) will vary with the layout placement of the device. A typical metal run capacitance (C_M) value is 0.14 picofarads.

D. As shown in Fig. 219, the metal gate over a device channel is 0.5 mil long (to cover channel length of 0.3 mil plus an overlap of 0.1 mil on each side allowing for mask registration tolerances during manufacture). A typical value of the gate metal oxide capacitance (C_G) is 1.7 picofarads. Summing up all the above capacitance values, the total fixed (i.e., static) input capacitance (C_F is approximately 5 picofarads.

$$C_{bp} + C_p + C_r + C_D + C_M + C_G = C_F$$

$$0.004 + 1 + 0.56 + 2 + 0.14 + 1.7 = 5 \text{ picofarads}$$

Dynamic Capacitance

The overlap of the gate metal over the drain diffusion shown in Fig. 219 and schematically in Fig. 220 represents the feedback portion of the gate capacitance coupled from the drain (output) to gate (input). During switching, the Miller effect brings about an increase in feedback capacitance proportional to the product of the device transconductance (g_m) and the static feedback capacitance (C_{DG}) as shown in Fig. 221.

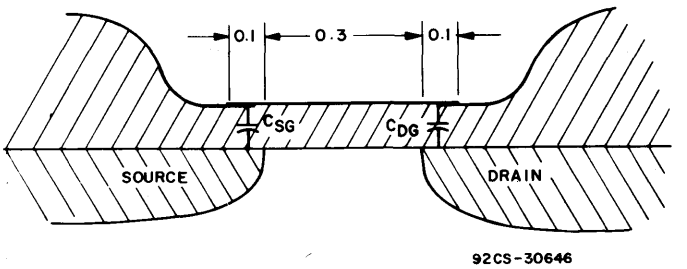


Fig. 219 – Dimensions of metal gate over device channel.

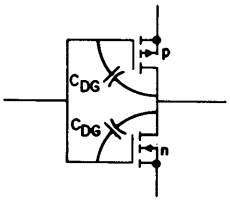


Fig. 220 – Feedback portion of metal gate capacitance.

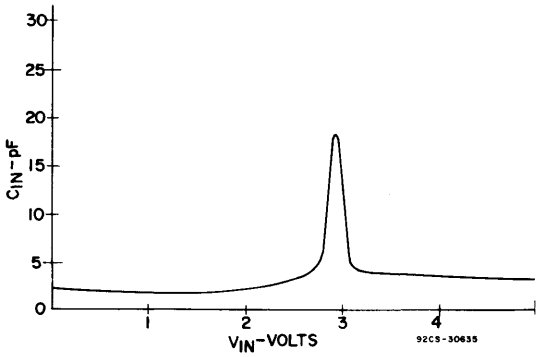


Fig. 221 – Capacitance increase caused by product of device transconductance and static feedback capacitance.

Although the curve in this figure peaks at a value of 5-10 times the fixed input capacitance (C_F), substitution techniques have established the true effective dynamic capacitance as approximately three times the static capacitance. The effect of this increased capacitance on device transition time should be taken into account in high-speed switching circuits. Fig. 222 illustrates the effect of increased capacitance on edge shape.

FABRICATION OF COS/MOS INTEGRATED CIRCUITS

All the COS/MOS circuits discussed in this Manual are monolithic integrated circuits. The distinguishing feature of any monolithic integrated circuit is that all components required to perform a particular circuit function are combined and interconnected on a common substrate. The constituent elements of the resultant circuits lose their identities as discrete components, and the over-all circuits, in essence, become microminiaturized function blocks. The monolithic technology, which makes possible simultaneous fabrication of conglomerates of solid-state devices within or on a very small chip of semiconductor material (usually silicon), is essentially an extension of the basic planar technology used in the fabrication of discrete silicon transistors.

The manufacture of silicon monolithic integrated circuits involves a series of highly critical operations in which silicon is subjected to carefully controlled, high-temperature chemical processes. The lateral physical dimensions of the chemical reactions in the silicon are controlled by photolithographic techniques. In the manufacture of monolithic integrated circuits, high-precision photomasks represent the assembly tools, jigs, and fixtures.

General IC Wafer Processing

Monolithic integrated circuits are not fabricated singly, but rather "by the wafer" as a minimum "batch". The fabrication process involves a sequence of diffusion and photolithographic engraving steps. Individual silicon wafers are cut from a silicon ingot into slices. Each wafer is then polished to a mirror finish. Circuit complexity determines the size of the chip for a particular design. Circuits being produced today use chip sizes up to about 240 mils square. For this range of chip sizes, the number of chips produced per wafer varies from the order of 1,000 down to about 100. Because the cost of processing a wafer is the same regardless of the number of chips it produces, it is evident that small chip area reduces the cost of the individual chips. In addition, defects tend to be random in

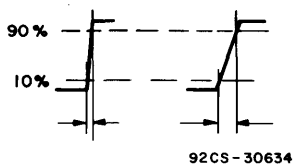


Fig. 222 – Effect of increased capacitance on edge shape.

nature. As a result, the probability of a defect is larger for a large chip area than for a small one. Thus, a smaller chip area increases processing yields and further reduces costs.

The first major step in processing the mirror-finished wafer involves the formation of a silicon dioxide layer on the surface of the wafer, as shown in Fig. 223. This thin layer of silicon dioxide protects the silicon surface

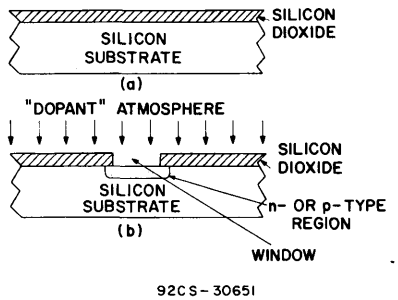


Fig. 223(a) — Formation of the silicon-dioxide layer on the surface of a wafer; (b) — layer used as mask.

of the finished integrated circuit, acts as a barrier to dopants during the semiconductor junction-forming processes, and provides an insulating substrate for the interconnection metals. Silicon dioxide is formed on the silicon wafer by heating it to a temperature of 1000 to 1300°C and passing oxygen over the surface. The silicon dioxide layer also serves as a "pattern mask" in determining the area through which "dopant" atoms may pass freely into the silicon substrate to form regions of either n-type or p-type silicon (depending on the type of dopant material used).

The ability to control the procedures by which "windows" are formed selectively in the silicon dioxide layer is one of the most crucial in integrated-circuit manufacturing. In some instances, the windows may be in the order of only 0.1 mil square. The windows in the silicon dioxide define the geometrical areas in which chemical diffusion reactions are localized. These windows are mechanically positioned and dimensioned by the use of **photomasks** and photochemical procedures, a system of processing which is dependent on the photosensitive properties of a type of lacquer called **photoresist.**

Fig. 224(a) illustrates the manner in which an oxide-coated silicon wafer is covered with a layer of photoresist lacquer several thousand angstroms thick. A photomask, in

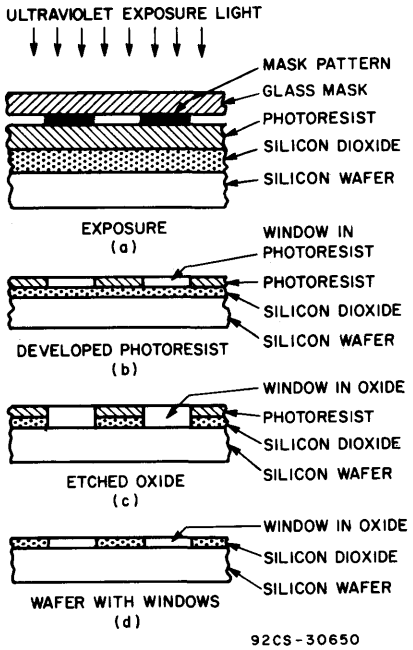


Fig. 224 — Photoresist processing of monolithic integrated-circuit wafer.

this case a glass plate having a pattern of black spots on it, is placed against the photoresist, and the system is exposed to ultraviolet light. Illuminated areas of the photoresist tend to harden (polymerize), while the areas under the black spots of the photomask remain soft and are removed during a subsequent "photo-development" operation. Fig. 224(b) shows the "exposed" patterns of the windows in the photoresist following the "photo-development" operation. The wafer is then subjected to a chemical **etchant** (such as diluted hydrofluoric acid), which dissolves the silicon oxide in the photoresist windows without attacking the silicon underneath. The desired windows in the silicon oxide are thus produced, as shown in Fig. 224(c). The remaining photoresist is removed chemically. This "cleaned" wafer, Fig. 224(d), with windows in its oxide coating is then ready for chemical doping procedures using ion implantation **diffusion** furnaces to produce regions with either n-type or p-type electrical

characteristics in the areas beneath the windows.

Chemical diffusion processes are used to introduce the semiconductor junction-forming dopants into the bulk silicon. A series of these diffusion cycles is performed in processing of integrated-circuit wafers.

COS/MOS IC Wafer Processing

The starting material (substrate) for a monolithic COS/MOS integrated circuit consists of a uniform single crystal of n-type silicon. Diffusion processing techniques (doping) permit introduction of certain impurities to desired depths and surface concentrations. Vertical penetration of the impurities is controlled by the diffusion temperature and time; control of lateral diffusion is made possible by a combination of the masking properties of silicon dioxide and photochemical techniques. The silicon-dioxide insulating material on the surface of the substrate is selectively opened (windows are formed) for each diffusion step. The oxide is subsequently replaced except in metal-contact areas.

Basic Device Formation and Interconnection Processes

The following paragraphs summarize the basic processes involved in the formation and interconnection of electronic components on a basic COS/MOS integrated circuit, such as the one shown in Fig. 225. The fabrication of a simple n-channel and p-channel device pair with gate protection is described.

As the initial step in the formation of a COS/MOS IC, p-type material is diffused vertically into the n-type substrate to form p-type regions (p-wells) in which the n-channel MOS device will be located. This initial step is shown in Fig. 226. Low-resistance p^+-type pockets, such as those shown in Fig. 227, are diffused into the n-type substrate to form the source and drain regions of the p-channel devices and into the well (p^- region) to form guard bands for n-channel devices. Low-resistance n^+-type pockets, like those shown in Fig. 228, are diffused into the p-well regions to form the source and drain regions of the n-channel devices and into the substrate to form guard bands for p-channel devices. As has been described, silicon dioxide (SiO_2) is necessary in integrated-circuit processing as a diffusion mask. However, in MOS processing, SiO_2 plays an

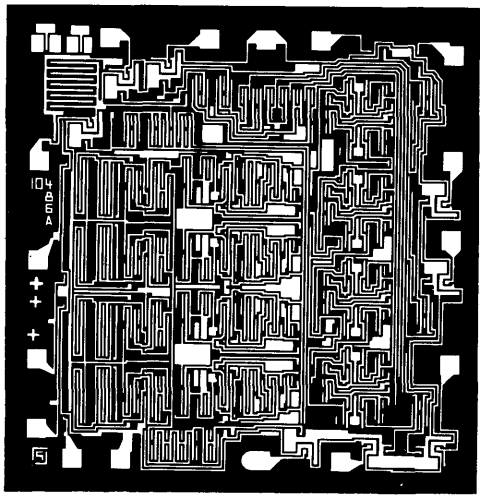


Fig. 225 – Photograph of a COS/MOS integrated circuit.

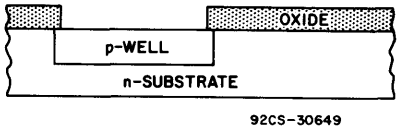


Fig. 226 – Formation of p-type regions in which n-channel MOS devices will be located.

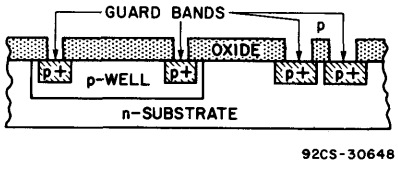


Fig. 227 – Low-resistance P^+-type pockets in the n-type substrate.

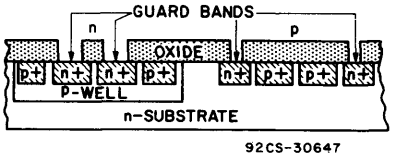


Fig. 228 – Low-resistance n^+-type pockets in the p-well region.

additional and more important role as a dielectric used to cover the channel region and insulate it from the metal gate. The processing technology by means of which a suitable oxide layer is obtained is the key to fabricating MOS devices.

It has been found that SiO_2 usually contains some ion contamination (most often sodium ions), and that these ions are positively charged. The positive charge carried by the ions can affect the characteristics of MOS devices significantly. In many instances this charge is fixed; in others, it is movable when stressed with voltage at elevated temperatures. The presence of a movable charge is very undesirable because it can cause serious problems in device stability and reliability. Therefore, clean-oxide technology has been developed to eliminate the contamination. This technology has made possible the fabrication of reliable n-channel and p-channel enhancement devices and thus is responsible for the development of the complementary-symmetry arrangement in integrated MOS devices.

Another important use of SiO_2 in MOS integrated circuits is as a **field oxide**, a thick oxide that insulates all non-active regions of the MOS IC from the interconnection metal. This insulation is needed to raise the threshold voltage of the inactive regions to a level beyond the operating voltage of the system so that undesired leakage currents are eliminated. The threshold voltage of the field oxide is usually referred to as the field threshold voltage.

Metallization of Completed Wafers

The series of oxidation and diffusion operations culminates in an integrated-circuit wafer that contains the desired electronic elements. High-conductivity metallic paths are then needed to interconnect these elements. The process by which these paths are fabricated is called metallization.

The metallization process is comprised of metal deposition, interconnection pattern delineation, and alloying. Metal deposition is performed by placing the processed wafer in a vacuum of about 10^{-6} torr (10^{-9} atmosphere). The source material (usually aluminum), which is also in the vacuum chamber, is then heated above its vaporization point by an electron beam heating source. As a result, metal is released by vaporization and condensed on the integrated-circuit wafer, coating it completely to a controlled thickness. The metal-coated wafer is then subjected to photolithographic procedures, including application of photoresist lacquer, exposure to ultraviolet light through a photomask having the desired pattern, and the removal of unwanted metal by acid etching. The resulting interonnnection patterns are similar to that shown in Fig. 229. Finally, in order to assure excellent electric contact between the aluminum and the electronic elements, the metallized wafers are heated in a furnace for a controlled period to permit a slight alloying of the aluminum with the semiconductor junctions.

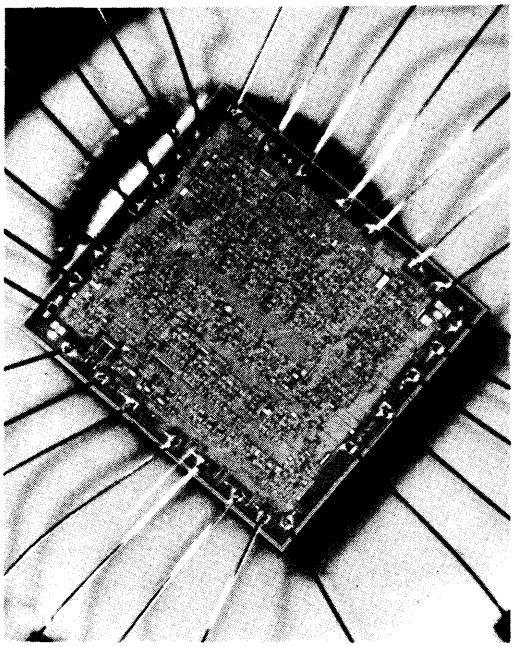


Fig. 229 — Integrated-circuit chip mounted with chip connected to package terminals.

Seven mask levels are normally used:

well
p^+
n^+
stepped oxide
contact
metal
protective glass

As shown in Fig. 225, the metallic interconnections terminate at the edges of the integrated-circuit chip as pads to which very fine wires connect the chip to the package terminals as shown in Fig. 229.

Probe Testing of Metallized Wafers

Elaborate automatic equipment has been developed to test chips while they are constituents of a complete wafer. The test procedure is frequently called "wafer-probing". A large number of needle-tipped probes make simultaneous electrical contact with the aluminum electrode pads on each chip. The probing equipment is designed so that the wafer is indexed automatically, with the probes contacting the individual chips sequentially. A spot of ink is automatically placed on each chip which fails electrical test, so that it can be easily discarded after the wafer is separated into chips.

Assembly and Final Testing

After the probe testing of the wafer is completed, the individual circuit chips must be separated and assembled into integrated-circuit packages. The packaged devices are then subjected to hermeticity, environmental, and final electrical testing. The sequence of events employed for these operations is as follows:

Separation of Chips - The individual chips in a wafer are separated by a technique similar to that used in glass cutting. A fine diamond point is used to "scribe" the wafer with its constituent chip pattern. The actual separation into chips is accomplished by an operation called "dicing", which is simply a system of mechanical fixturing by which stress is applied to the wafer in such a manner that mechanical separations occur along the scribed lines. With new techniques, using a diamond saw blade or laser beam, both "scribing" and "dicing" are performed in a single operation. "Sorting" is the rejection of chips which were found to be defective in wafer-probing or dicing operations. Microscopic inspection of each chip is also performed to cull out circuits with visible imperfections.

Chip Bonding - In the bonding procedure, the chip is securely mounted in the package by means of a silver-filled conductive epoxy.

Lead Bonding - After the chip is firmly affixed in the package, electrical connections are made to the terminal-post leads. Aluminum wires of about 1.5-mil diameter are commonly used to make these connections. Recent development of accurate, computer-controlled equipment has led to "automatic bonding" systems.

Capping and Sealing - The lead-bonded chip assembly (header) is usually subjected to cleaning and vacuum bake-out operations prior to sealing. Actual hermetic sealing is accomplished by a variety of means, depending to some extent on the package design. Local application of heat (e.g., welding) is used to seal the cap to the package header. This step is conducted in a dry atmosphere. In the case of non-hermetic packages like plastic, the lead-bonded chip assembly is encapsulated in plastic or epoxy materials.

Hermeticity and Environmental Testing - Hermeticity testing is used to confirm the leak resistance of the package. The helium leak-detection technique is frequently used. In this method, completed packages are placed in an atmosphere of helium pressure for a period of time. Helium is able to penetrate through any imperfections which may exist in the package. After removal from the helium pressurization chambers, sensitive mass-spectrograph leak detectors are used to detect helium "oozing" out of any imperfection in the package.

Mechanical shock, vibration, acceleration, and thermal shock tests are used to screen out devices that have inadequate margins against anticipated stresses for the particular class of service in which the integrated circuit is to be applied.

Final Electrical Testing - Wafer-probing of COS/MOS integrated-circuit chips is usually limited to static parameter tests and dc functional tests because the length of probe leads and other factors prevent meaningful ac, rf, or pulse testing. Consequently, any ac testing required is performed on packaged units only. Test equipment presently used on COS/MOS integrated circuits is almost entirely automated.

CUSTOM DESIGNS

Creating the Layout Drawing

The major task in implementing a logic design as a custom LSI chip is the creation of the layout drawing. This drawing must show every transistor in the array (using color coding for the different levels) with all interconnections to the rest of the circuitry. As determined by load and speed requirements, the channel width for each transistor must be specified. (Except for high-impedance devices, channel length is fixed at 0.3 mil by punchthrough and processing considerations). Fig. 230 shows the layout of 16 transistors in a flip-flop; this figure represents a small portion of the layout drawing, because an average LSI array might have a total of 1500 transistors.

A firm set of design rules defines minimum spacing and sizes for diffusions, metal lines, oxide openings, etc. Because these rules are fixed by a combination of physical parameters (side diffusion, etch angles, light scattering) and processing technology (mask registration, run-out, photo-resist resolution) and have been established over a considerable period of COS/MOS device manufacture, no deviations can be allowed. Fig. 231 shows some design minimums for line widths and separations.

Master Making and Testing

Once the layout is completed and checked, each layer is "digitized"; this step converts all dimensions and lines on the drawing to numerical values which are stored in a computer memory. This digital information can be used to generate "pen-plots" for further checking of the layers and registration between layers. After checking and correcting, the digital data is used to drive a pattern-generator camera which creates a set of mask reticles. Each mask reticle represents one layer at ten times final size.

To generate the multiple patterns that enable many chips to be processed simultaneously on a single wafer, the reticles are placed in a "step-and-repeat" camera which exposes a master plate for each layer. Glass prints of the master, called working plates, are actually used in wafer processing.

Every custom-designed chip needs two special computer test programs. One is for a fast "functional" test for wafer probing to grossly screen out defective chips. The other is a complete program for final test of bonded and packaged units.

Functional Design Considerations

Before a logic design is implemented as a layout drawing, it should be reviewed from

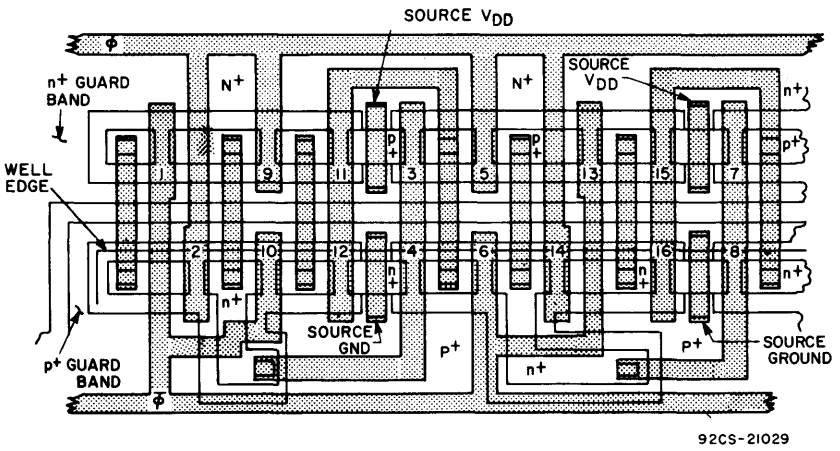


Fig. 230 – Typical layout for a "D"-type flip-flop circuit.

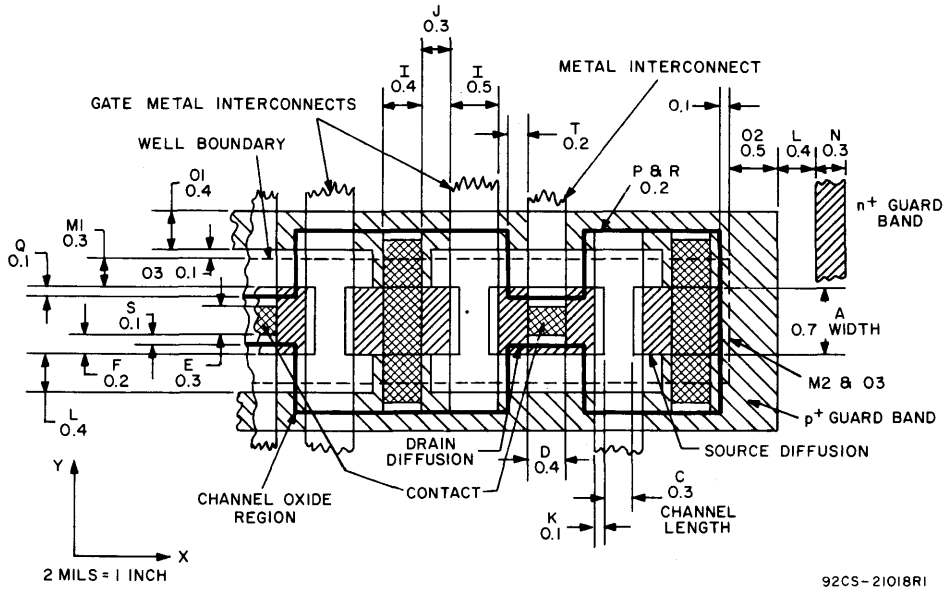


Fig. 231 – Typical design minimums for line widths and separations used in layout of COS/MOS IC arrays.

the point of view of minimizing the device count. Because of the differences between a logic design using "building-block" NAND and NOR gates and one which creates the same logic function using "tree" or "functional-gating" logic, the saving in devices can be considerable. As an example, Fig. 232 shows eight devices (four p and n pairs)

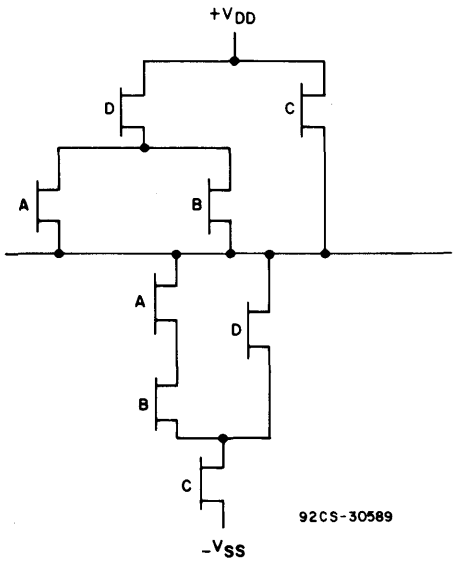


Fig. 232 – "Tree" or "functional gating" logic.

performing the same logical function as eighteen devices in Fig. 233. arranged as NAND and NOR gates. The savings would be 44%, translated directly into area savings on the chip.

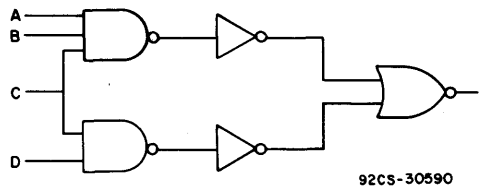


Fig. 233 – "Building-block" design using NAND and NOR gates.

The Boolean expression for this logic function is

$$\overline{A \cdot B \cdot C + C \cdot D}$$

Factoring the common term:

$$\overline{C(A \cdot B + D)}$$ (Apply to n devices)

Complementing for the p devices:

$(C + (A + B) \cdot D$ (Apply to p devices)

Note that all devices must be complemented, that is, each input signal must appear on the gates of both a p and an n device.

The engineering, drafting, and mask-making costs involved in a custom design must be balanced against the savings of the single chip in production volume over the cost of standard parts, including substrate board, assembly, interconnection, and test. Special considerations such as the importance of size (as in a wrist watch) or the improved reliability of an integrated circuit (intra-chip connections are more reliable than inter-chip connections) must also be evaluated. These factors can be discussed with an RCA Field Sales Representative who can provide cost information on the three techniques RCA has developed for custom designs: Universal Array, APAR (computer-controlled automatic placement and routing interconnections of standard cells), and Manual Layout. These three techniques are briefly discussed in the following material.

Gate Universal Array:

A Gate Universal Array consists of a fixed placement of p devices, n devices, and tunnels in a repetitive ordered structure on a silicon or sapphire substrate. All drains, sources, and tunnel ends are accessible. All the mask definition levels, except the metal mask, are fixed. The metal definition mask uniquely defines the device interconnect metal for each application. The Gate Universal Array Technique provides the following features: single mask definition, quick turnaround time, high reliability, low design cost, and the quick correction of errors or logic changes. It does not require that the user have processing experience or knowledge of IC layout design rules.

As shown in Table XIX, the Gate Universal Array is available in several sizes and technologies. As described in the **COS/MOS Array User's Manual** and in the **SOS COS/MOS Universal Array User's Manual**, there are three approaches at different interface levels that the designer may use. In the Level I approach, the customer supplies the required logic in any form together with other necessary specifications. In the Level II approach, the customer supplies a logic diagram annotated in Gate Universal Array logic cells as defined in the User's Manuals together with any other necessary specifications. In the Level III approach, the customer does the logic layout on special plastic sheets provided by RCA for that purpose and supplies an annotated logic diagram, test pattern, and other necessary specifications. In all three, RCA will fabricate, package, test, and deliver a quantity of working units.

The Gate Universal Array Technique emphasizes low initial design cost, quick turnaround time, and rapid error correction at the expense of a somewhat larger chip.

Table XIX – Summary of Gate Universal Array

Technology	Type No.	No. of Gates*	No. of Pads
Metal-Gate CMOS (MG COS/MOS)	TCC 040	168	40
	TCC 051	276	48
Silicon-Gate CMOS (C^2L COS/MOS)	TCC 220	168	40
	TCC 221	276	48
	TCC 222	410	48
	TCC 223	576	64
Silicon-Gate CMOS on Sapphire (SOS COS/MOS)	TCS 090	182	40
	TCS 091	300	48
	TCS 092	452	64
	TCS 093	632	64

*A gate consists of two p and two n devices and is the equivalent of a two-input gate.

APAR (Automatic Placement and Routing)

In the APAR technique (APAR is an acronym for Automatic Placement And Routing), a sophisticated computer program utilizing an extensive growing library of Standard Cells stored in memory optimizes the placement of cells so as to minimize the lengths of interconnecting metal runs. The library includes metal-gate, C^2L, and silicon-on-sapphire cells of either the single-ended or double-ended type. In the single-ended cells connections are made at one end; in the double-ended cells connections can be made at both ends thereby facilitating a more compact design. The program inputs are based on the Boolean expressions for the complete logical function of the array. A companion program generates the test programs.

APAR is more efficient in chip-area utilization than the Universal Array, but not as efficient as Manual Layout. The time period required to reach the working chip stage is considerably shorter than that of the Manual Layout technique. One of the reasons for this time advantage is the fact that APAR uses only Standard Library Cells. These Cells have proven themselves over many years of use so that almost all APAR arrays work on the first go-around.

Many customers use APAR to take advantage of its fast delivery cycle and moderate costs to build prototypes with integrated circuits as a final check on systems and product design. Then, before entering the high-production-volume stage, a more efficient Manual Layout design is made.

Manual Layout

For the Manual Layout Technique, an RCA specialist will review the customer's logic design, minimize device count and lead lengths, specify device sizes, and supervise the layout of the chip by an experienced draftsman. Because this approach provides the most compact array, and, consequently the highest potential yield per wafer, it should be used for high-volume circuits.

The computer test program is written while the masks are being made in RCA's in-house mask-making facility and a sample wafer run is then processed. Wafers are tested, debugged if necessary, and engineering samples supplied for customer evaluation.

If the customer chooses to create his own layout design, he should make an intensive study of the COS/MOS custom layout practices as a first step.

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